

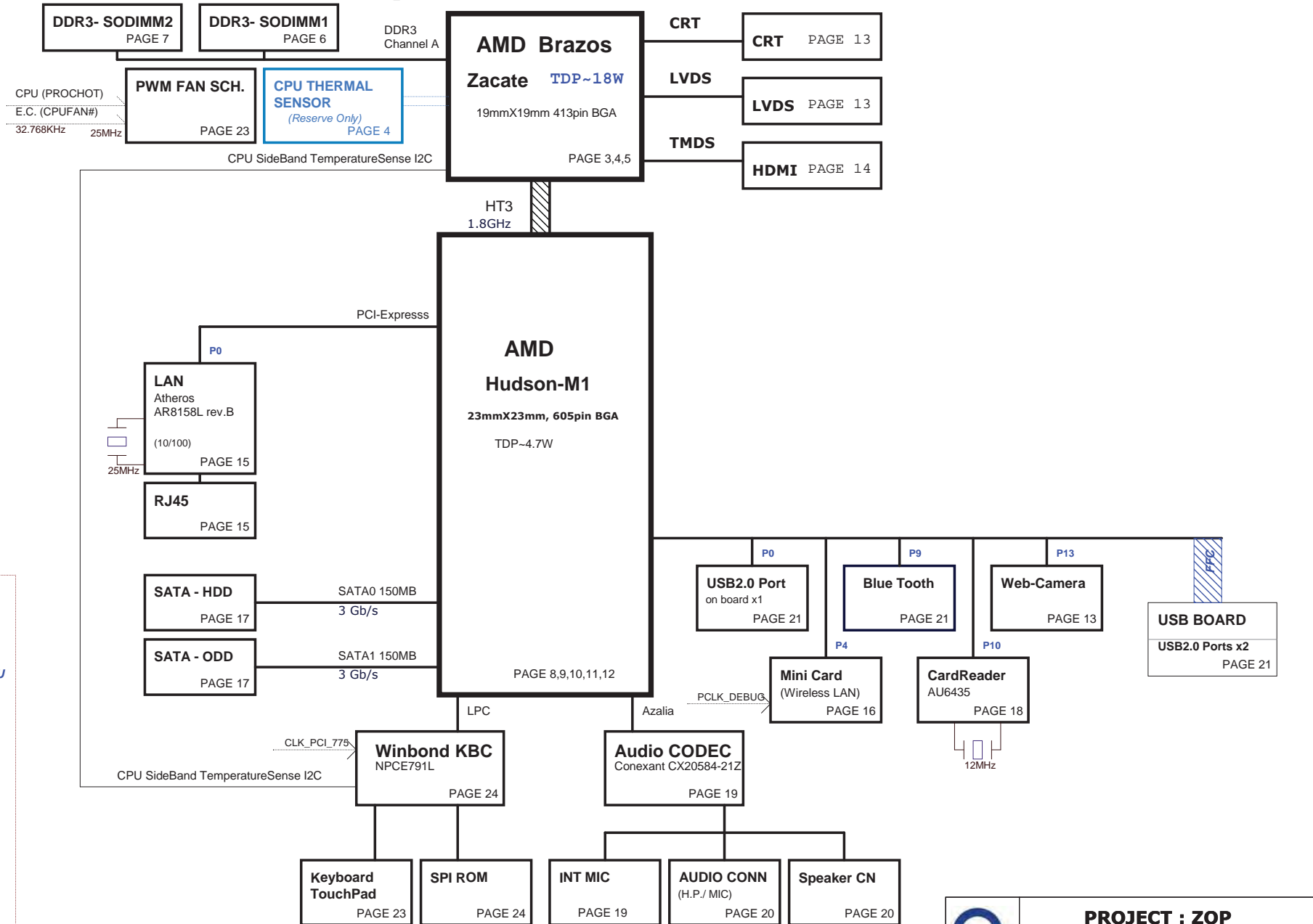
ZQP SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

HDMI@ -----> HDMI option
SP@ -----> Board ID/Strap pin
H@ -----> 家電下鄉

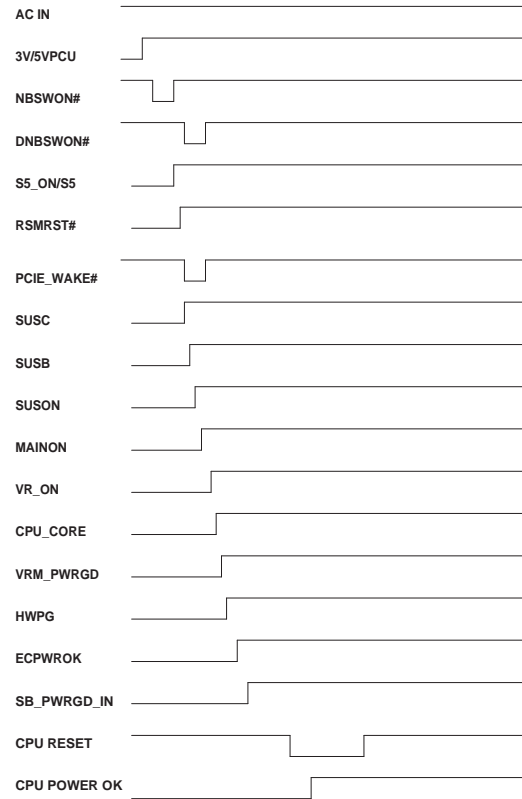
UMA REV:B



CHARGER (ISL88731A)	PAGE 25	
AMD CPU CORE (OZ8380)	PAGE 27	CPU
1V (G5602)	PAGE 29	NB
0.9V/DDR 1.5V(RT8207)	PAGE 37	
SYSTEM 5V/3V (RT8223M)	PAGE 26	
1.1V(G5602)	PAGE 28	
Discharge /Thermal protec	PAGE 31	

PAGE#	DESCRIPTION	NOTE
1	BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	ONTARIO MEM & PCIE I/F(1/3)	
4	ONTATIO DISPLAY/CLK/M(2/3)	
5	ONTARIO POWER & DECOUP(3/3)	
6	DDR3 SO-DIMM (STD=8)	
7	DDR3 SO-DIMM (STD=4)	
8	HUDSON PCIE/LPC/CPU IF(1/5)	
9	HUDSON ACPI/GPIO/USB(2/5)	
10	HUDSON SATA/BIDs(3/5)	
11	HUDSON PWR/GND(4/5)	
12	HUDSON STRAPS/PWRGD(5/5)	
13	CRT/LVDS/CCD	
14	HDMI	
15	LAN AR8152	
16	MINI PCI-E	
17	HDD /ODD	
18	CARD READER	
19	AUDIO - CONEXANT 20584	
20	AUDIO JACK CONN	
21	USB / BT /TP	
22	LED / NUT	
23	KB/FAN/TP	
24	WPCE791 /FLASH	
25	CHARGER (ISL88731A)	
26	SYSTEM 5V/3V (RT8223M)	
27	CPU CORE (OZ8380)	
28	VCCP 1.1V (G5602)	
29	+1V(G5602)	
30	DDR 1.5V (RT8207A)	
31	+1.8V/Discharge/Thermal Protection	
32	Change list	

Power Sequence

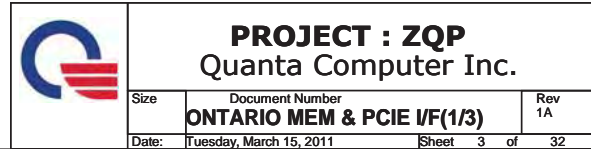


Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

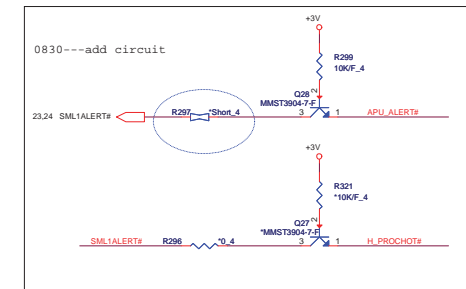
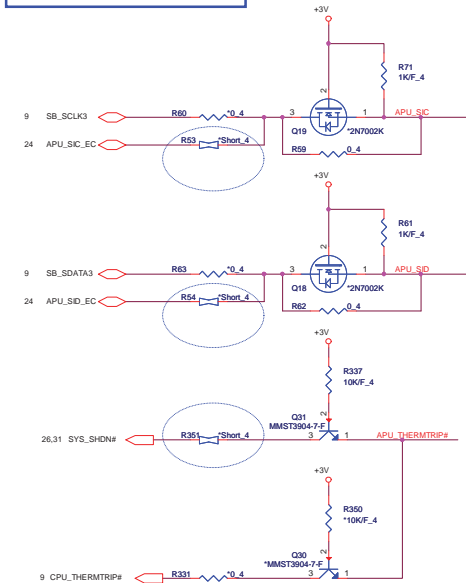
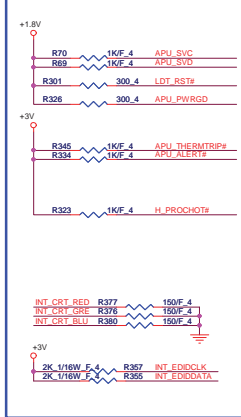
KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

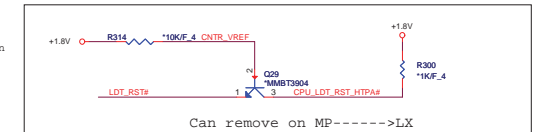
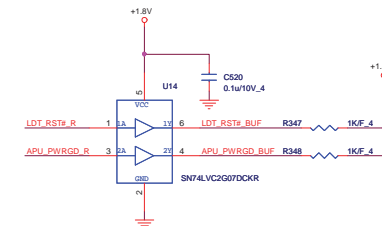
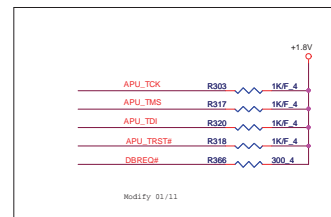
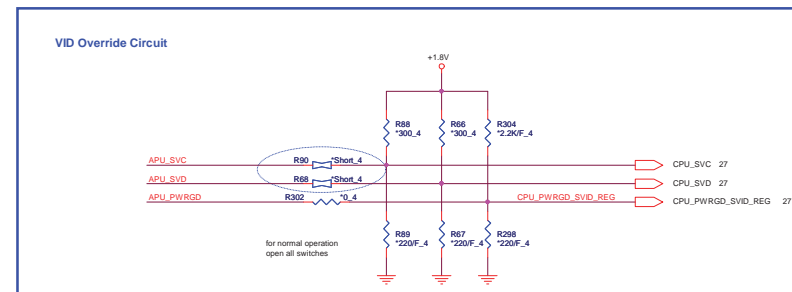
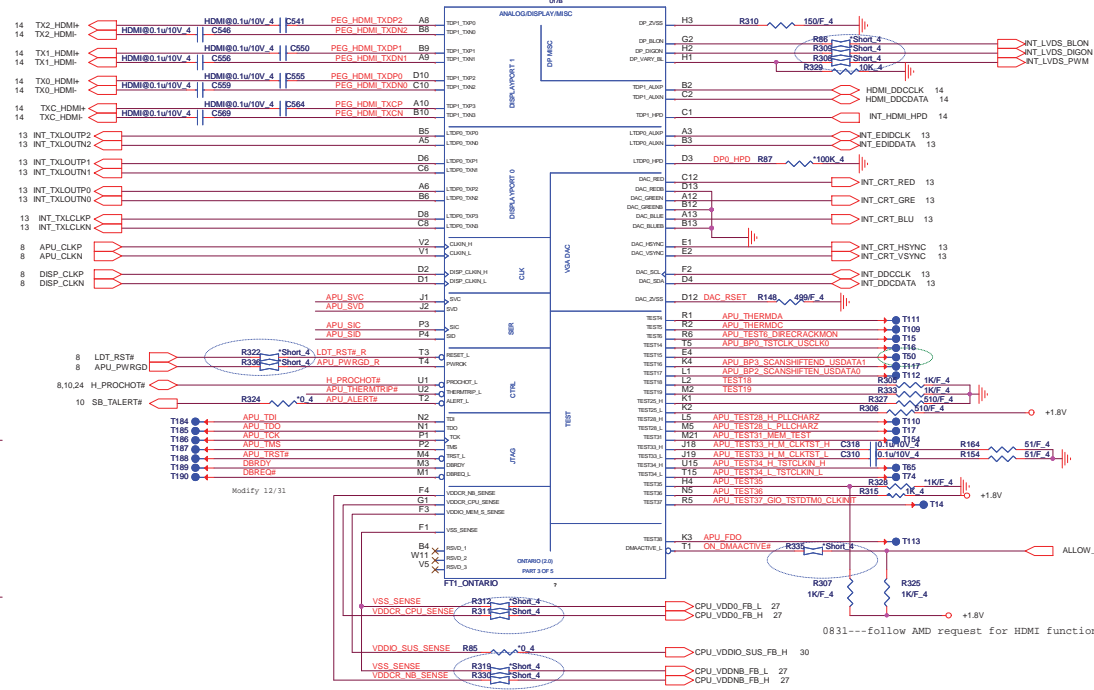


E350	AJ0E350VT01
C50	AJ00C50VT02

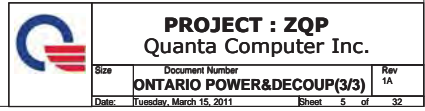
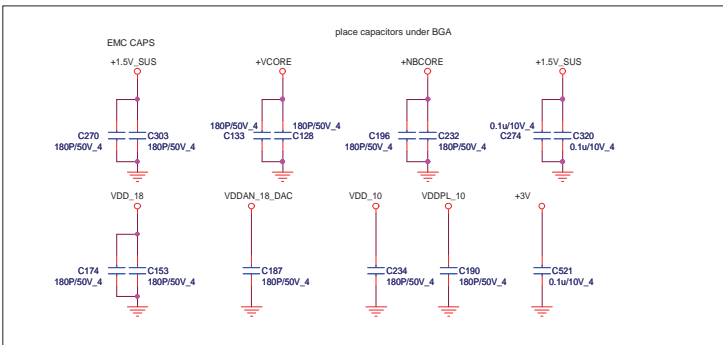
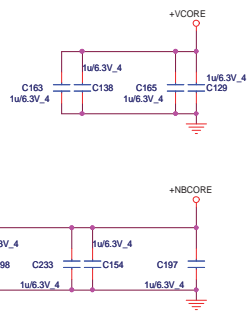
+1.8V 5.31
+3V 5.6,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31





AGS HDMI 01/18

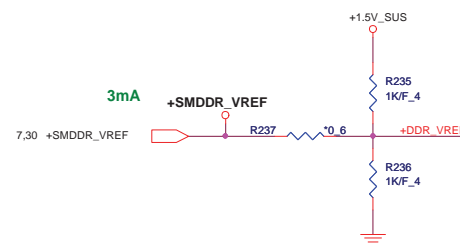
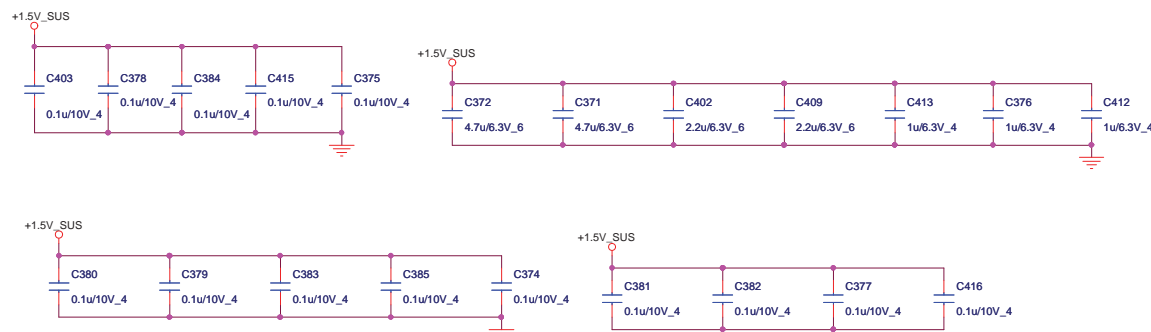
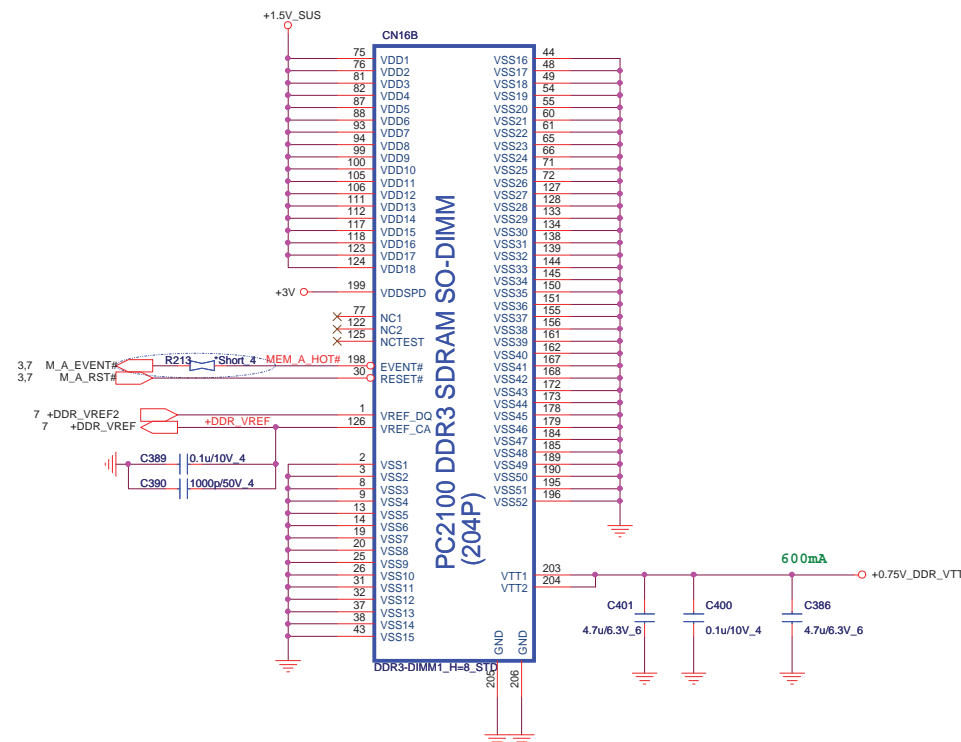
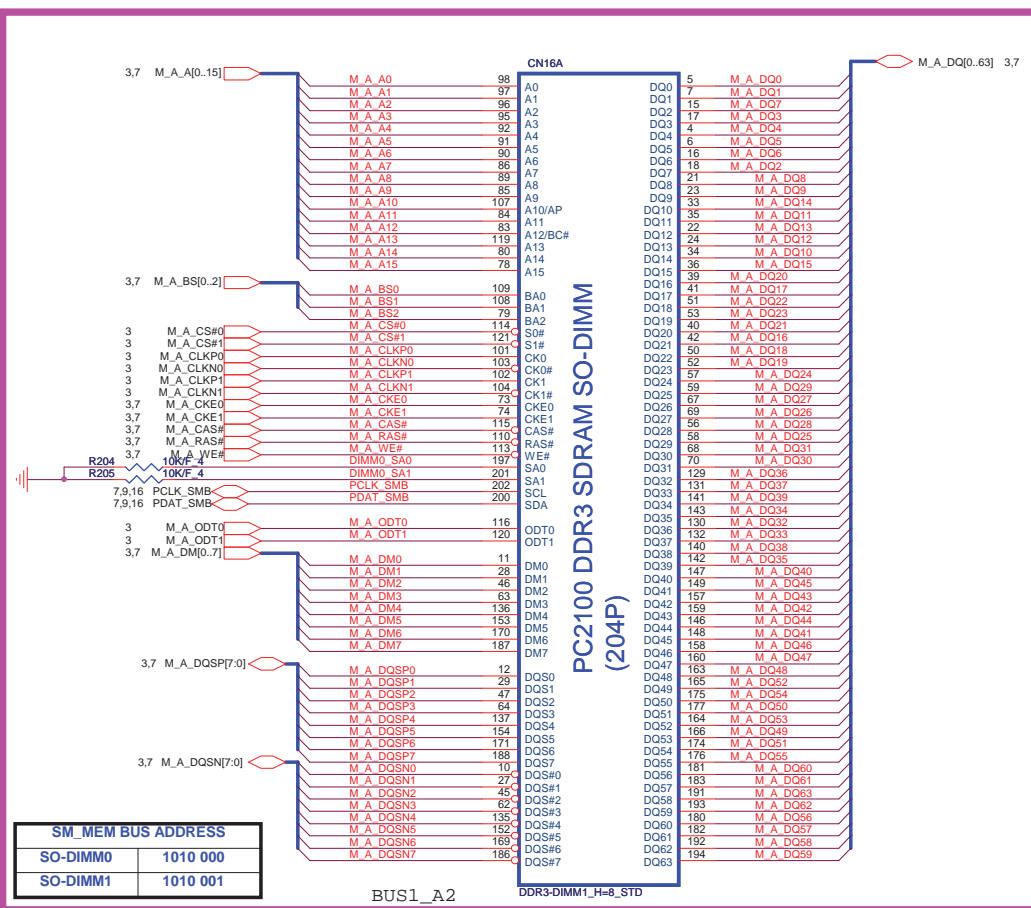


PROJECT : ZQP Quanta Computer Inc.			
Size	Document Number	Rev	1A
ONTARIO DISPLAY/CLK/M(2/3)			
Date:	Tuesday, March 15, 2011	Sheet	4 of 32



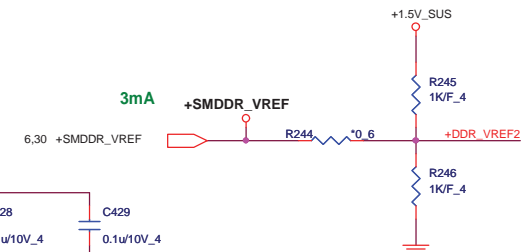
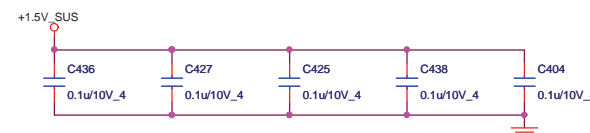
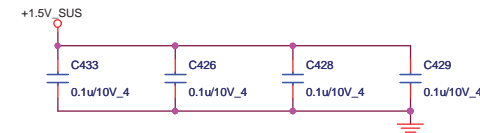
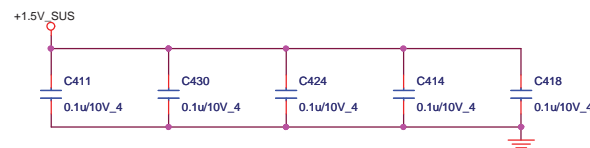
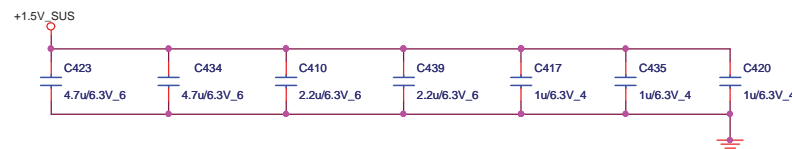
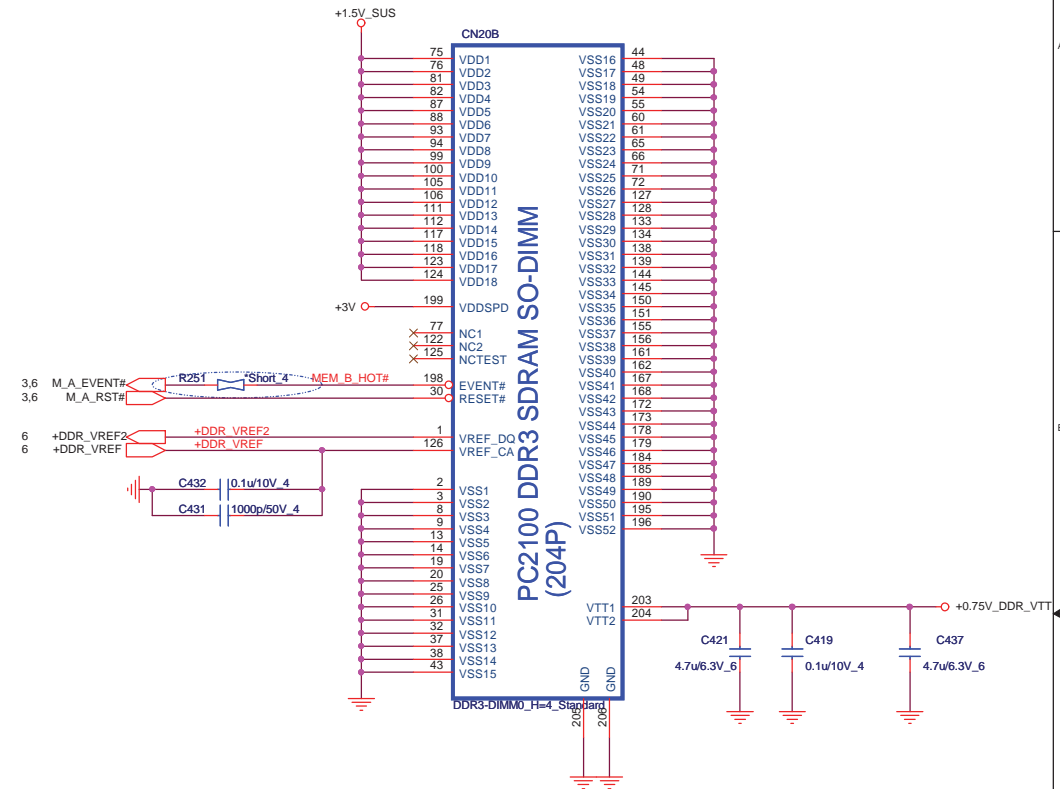
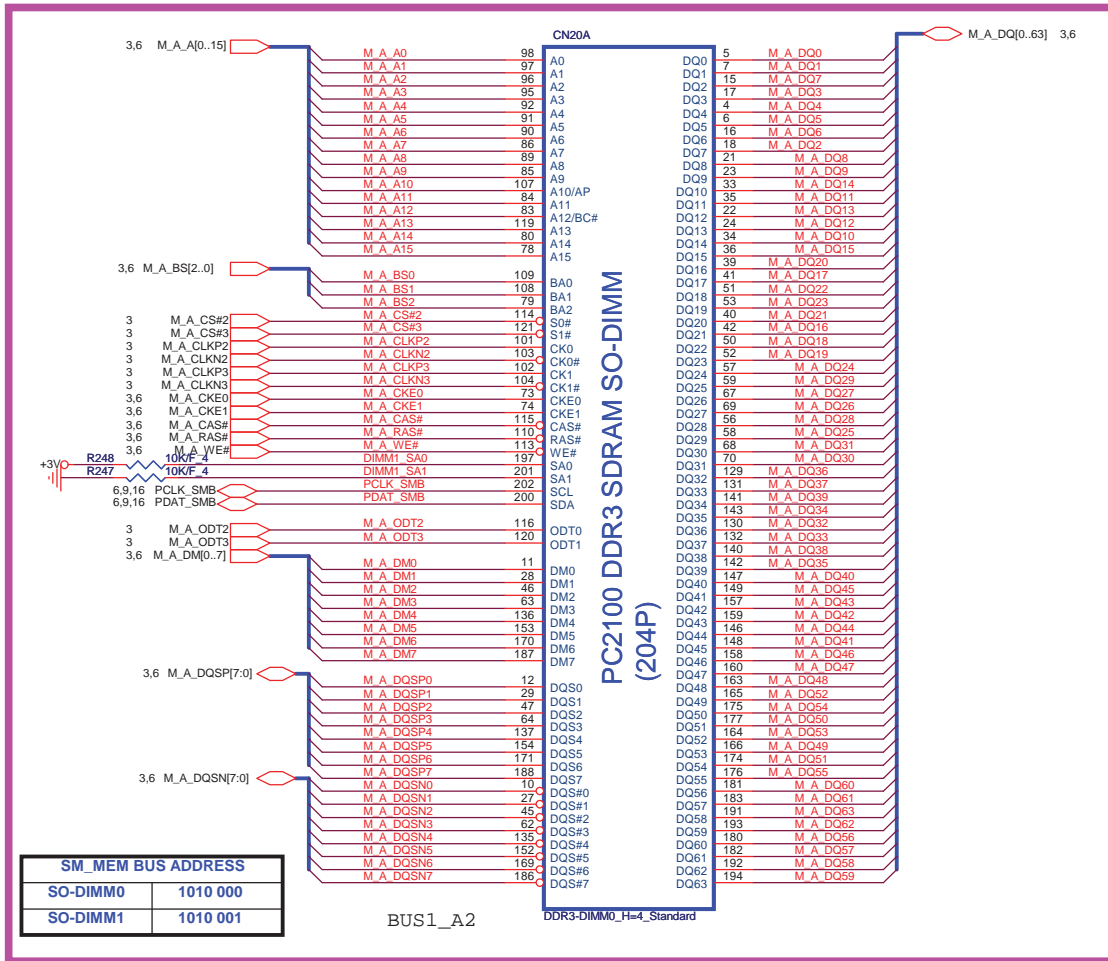
0830--P/N and footprint are follow ZR7B

 +1.5V_SUS 3,5,7,22,30
 +0.75V_DDR_VTT 7,30
 +3V 4,5,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31



PROJECT : ZQP
Quanta Computer Inc.

Size: Document Number
DDR3 SO-DIMM (STD)
 Date: Tuesday, March 15, 2011 Sheet 6 of 32



[illegible]

BG625000486

CR2032 (Non-Chargeable)
 AHL03003014
 AHL030M0009

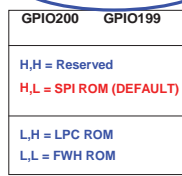
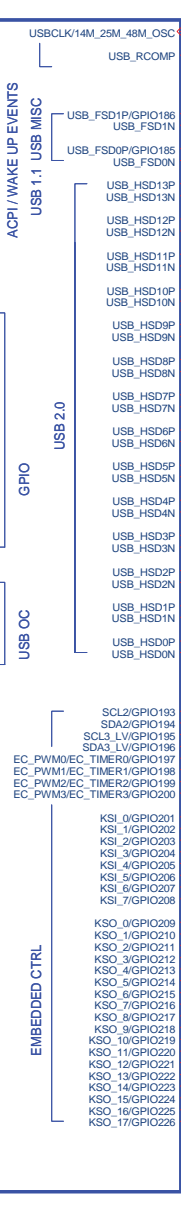
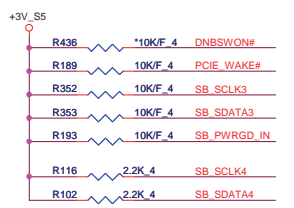
[illegible]

RTC_CLK must ready before RSMRST#

PCH_SUSCLK

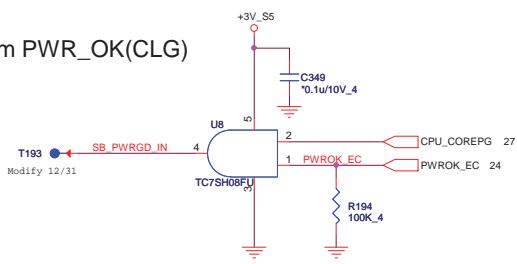


Size	Document Number	Rev
	HUDSON PCIE/LPC/CPU IF(1/5)	1A
Date:	Tuesday, March 15, 2011	Sheet 8 of 32



GPIO199 R162 *2.2K 4
GPIO200 R134 2.2K 4

has checked with
AMD FAE already--Allen





SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON M1

SATA HDD

SATA ODD

PLACE SATA CAL RES
VERY CLOSE TO BALL
OF HUDSON M1

XTLVDD SATA-- SATA
crystal power
PLVDD SATA--
SATA PLL
POWER

AVDD_SATA

22 SATA_LED#

C575

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AVDD_SATA

22 SATA_LED#

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AVDD_SATA

22 SATA_LED#

C575

C582



This page is different AMD Nile

Hudson M1

Pin	Signal	Pin	Signal	Pin	Signal
Y14	VSSIO SATA_1	VSS_1	AJ2		
Y16	VSSIO SATA_2	VSS_2	A28		
AB16	VSSIO SATA_3	VSS_3	A2		
AC14	VSSIO SATA_4	VSS_4	E5		
AE12	VSSIO SATA_5	VSS_5	D23		
AE14	VSSIO SATA_6	VSS_6	E25		
AF9	VSSIO SATA_7	VSS_7	F24		
AF11	VSSIO SATA_8	VSS_8	F15		
AF13	VSSIO SATA_9	VSS_9	R13		
AG8	VSSIO SATA_10	VSS_10	R17		
AH7	VSSIO SATA_11	VSS_11	T10		
AH11	VSSIO SATA_12	VSS_12	P10		
AH13	VSSIO SATA_13	VSS_13	V11		
AH16	VSSIO SATA_14	VSS_14	U15		
AJ7	VSSIO SATA_15	VSS_15	M18		
AJ11	VSSIO SATA_16	VSS_16	V19		
AJ13	VSSIO SATA_17	VSS_17	M11		
AJ16	VSSIO SATA_18	VSS_18	L12		
	VSSIO SATA_19	VSS_19	L18		
		VSS_20	J7		
A9	VSSIO USB_1	VSS_21	P3		
B10	VSSIO USB_2	VSS_22	V4		
K11	VSSIO USB_3	VSS_23	AD6		
B9	VSSIO USB_4	VSS_24	A04		
D10	VSSIO USB_5	VSS_25	AB7		
D11	VSSIO USB_6	VSS_26	AC9		
D14	VSSIO USB_7	VSS_27	V8		
F14	VSSIO USB_8	VSS_28	W9		
E9	VSSIO USB_9	VSS_29	B9		
F9	VSSIO USB_10	VSS_30	A120		
F12	VSSIO USB_11	VSS_31	J23		
F16	VSSIO USB_12	VSS_32	U4		
C9	VSSIO USB_13	VSS_33	Y18		
G11	VSSIO USB_14	VSS_34	Y10		
G11	VSSIO USB_15	VSS_35	Y12		
F18	VSSIO USB_16	VSS_36	Y11		
D8	VSSIO USB_17	VSS_37	AA11		
H12	VSSIO USB_18	VSS_38	AA12		
H14	VSSIO USB_19	VSS_39			
H18	VSSIO USB_20	VSS_40			
J11	VSSIO USB_21	VSS_41	J4		
J11	VSSIO USB_22	VSS_42	G8		
K14	VSSIO USB_23	VSS_43	G9		
K19	VSSIO USB_24	VSS_44	AF25		
K16	VSSIO USB_25	VSS_45			
K16	VSSIO USB_26	VSS_46	H27		
H19	VSSIO USB_27	VSS_47	Y10		
	VSSIO USB_28	VSS_48	P6		
		VSS_49	N4		
		VSS_50	L8		
Y4	EFUSE	VSS_51	L4		
		VSS_52			
D8	VSSAN_HW11				
M19	VSSXL	VSSPL_SYS	M20		
P21	VSSIO_PCIECLK_1	VSSIO_PCIECLK_14	H23		
P21	VSSIO_PCIECLK_2	VSSIO_PCIECLK_15	H26		
M22	VSSIO_PCIECLK_3	VSSIO_PCIECLK_16	AA21		
M24	VSSIO_PCIECLK_4	VSSIO_PCIECLK_17	AA23		
P22	VSSIO_PCIECLK_5	VSSIO_PCIECLK_18	AB23		
M26	VSSIO_PCIECLK_6	VSSIO_PCIECLK_19	AD23		
P26	VSSIO_PCIECLK_7	VSSIO_PCIECLK_20	AA26		
T20	VSSIO_PCIECLK_8	VSSIO_PCIECLK_21	AC26		
T20	VSSIO_PCIECLK_9	VSSIO_PCIECLK_22	W21		
T24	VSSIO_PCIECLK_10	VSSIO_PCIECLK_23	W20		
V20	VSSIO_PCIECLK_11	VSSIO_PCIECLK_24	AE26		
V20	VSSIO_PCIECLK_12	VSSIO_PCIECLK_25	L21		
J23	VSSIO_PCIECLK_13	VSSIO_PCIECLK_26	K20		
		VSSIO_PCIECLK_27			

Part 5 of 5

PROJECT : ZQP
Quanta Computer Inc.

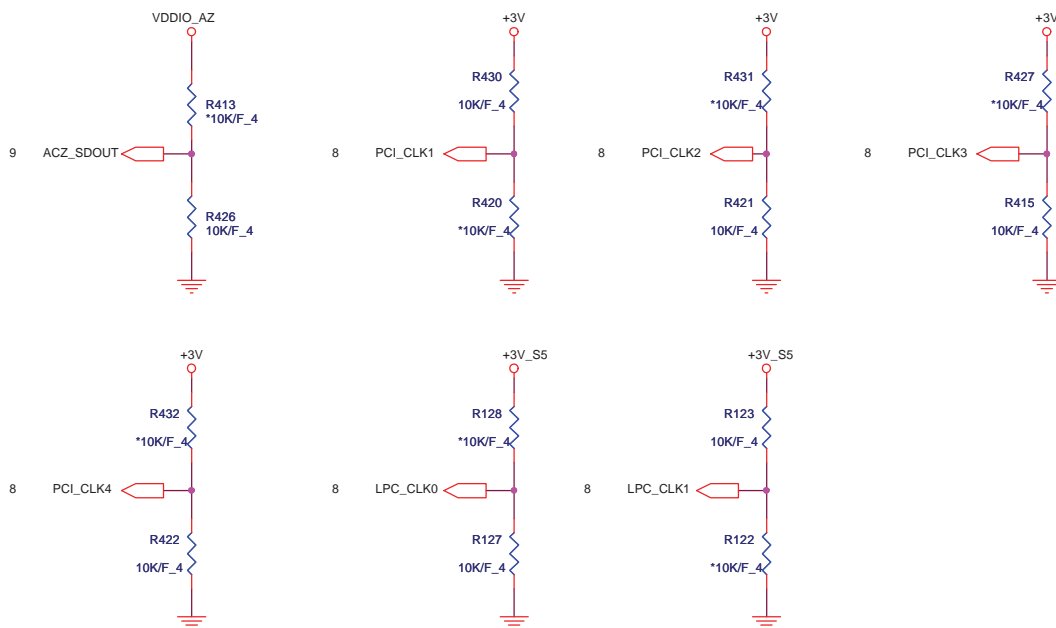
Size	Document Number HUDSON PWR/GND(4/5)	Rev 1A
Date:	Tuesday, March 15, 2011	Sheet 11 of 32



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

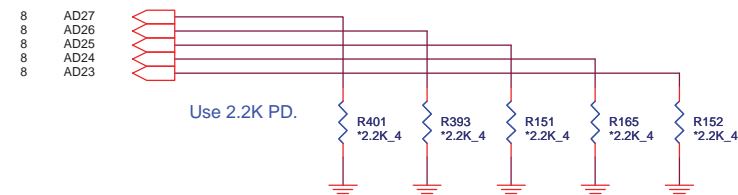


VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,10,11,15,21,22,26

12

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



PROJECT : ZQP
Quanta Computer Inc.

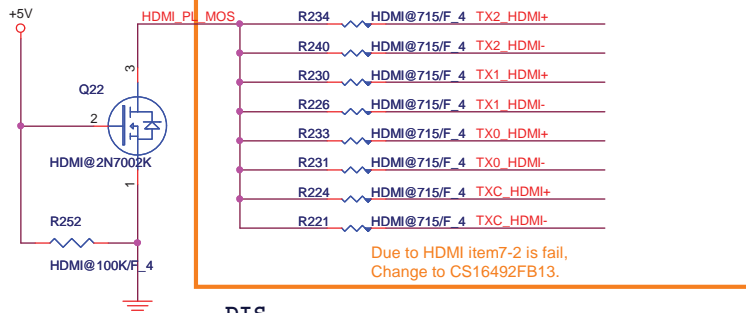
Size	Document Number HUDSON STRAPS/PWRGD(5/5)	Rev 1A
Date:	Tuesday, March 15, 2011	Sheet 12 of 32

HDMI SDVO I2C Control



HDMI (HDM)

Close to HDMI Connector

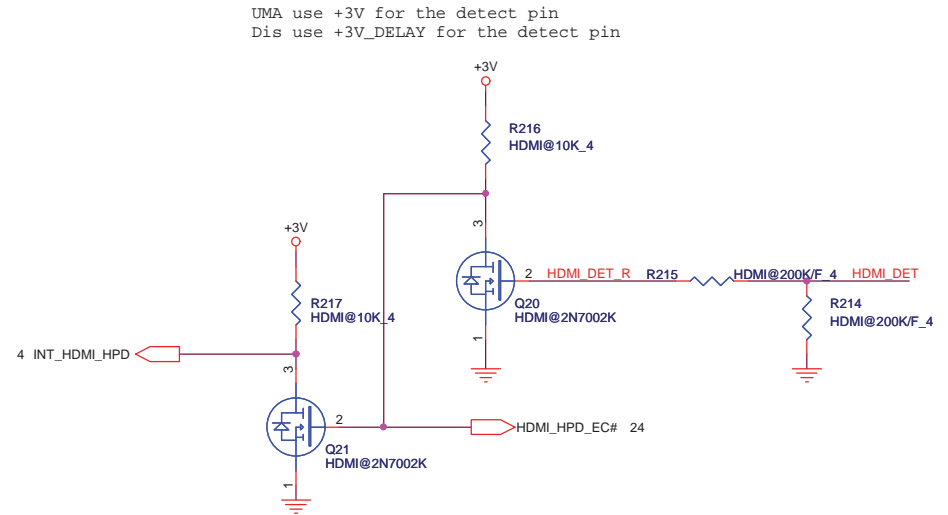
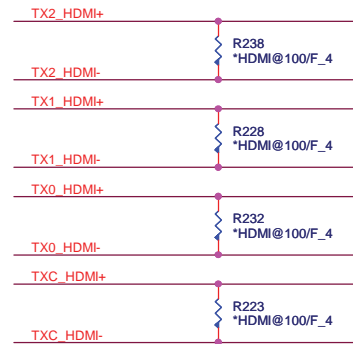


DIS
Stuff 499 ohm CS14992FB24



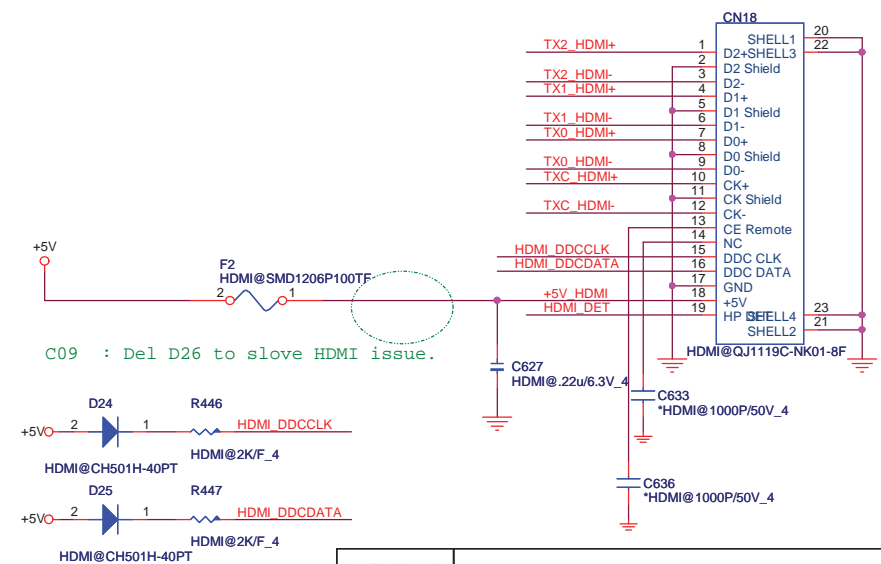
EMI reserve for HDMI(EMC)

Close connector



Added HDMI function
01/19 REV:B

HDMI PORT (HDM)



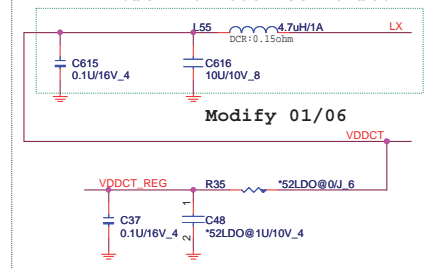
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI	1A
Date:	Tuesday, March 15, 2011	Sheet 14 of 32

<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

<Layout note>
Close to Pin1

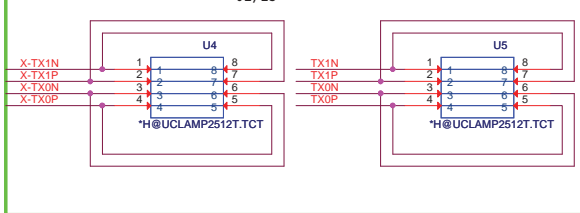
If use LDO mode L55 no stuff



Modify 01/06

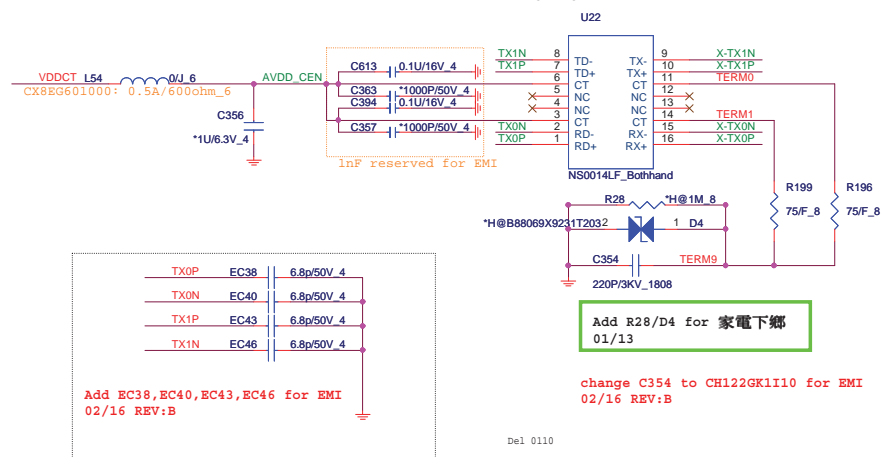
BG625000486

Add R28/D4 for 家電下鄉
01/13



TRANSFORMER (LAN)

exchange pair 0/1
0110



Del 0110

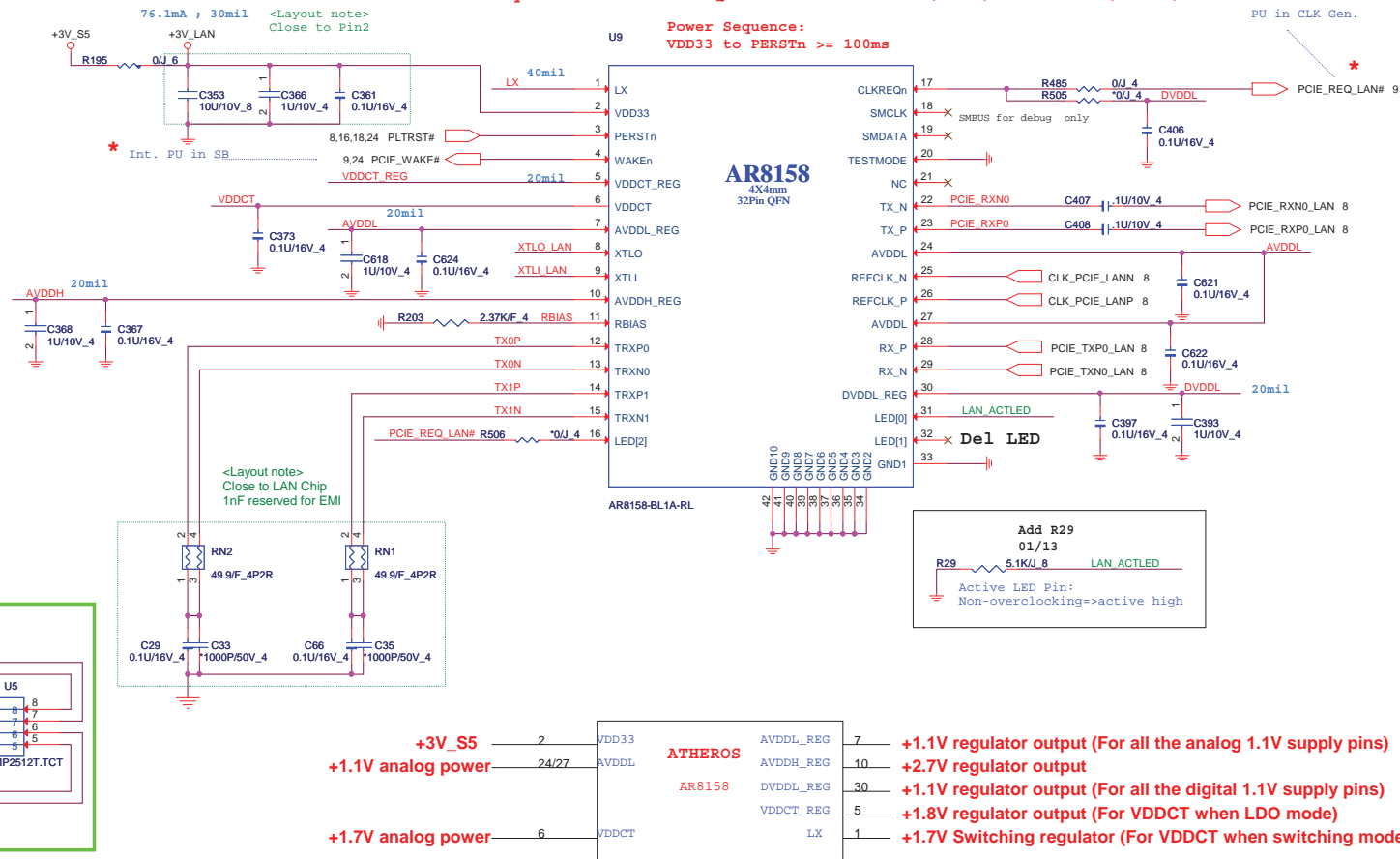
Add R28/D4 for 家電下鄉
01/13

change C354 to CH122GK110 for EMI
02/16 REV:B

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERSTn >= 100ms

AR8158
4X4mm
32Pin QFN

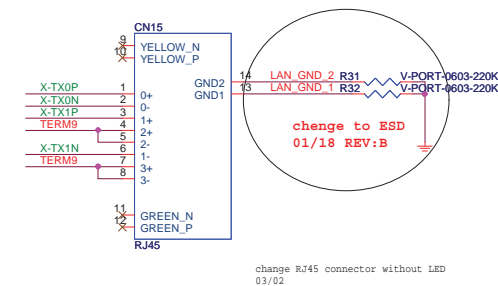


+3V_S5
+1.1V analog power
+1.7V analog power

+1.1V regulator output (For all the analog 1.1V supply pins)
+2.7V regulator output
+1.1V regulator output (For all the digital 1.1V supply pins)
+1.8V regulator output (For VDDCT when LDO mode)
+1.7V Switching regulator (For VDDCT when switching mode)

RJ45 Connector (LAN)

Del LAN LED 01/05



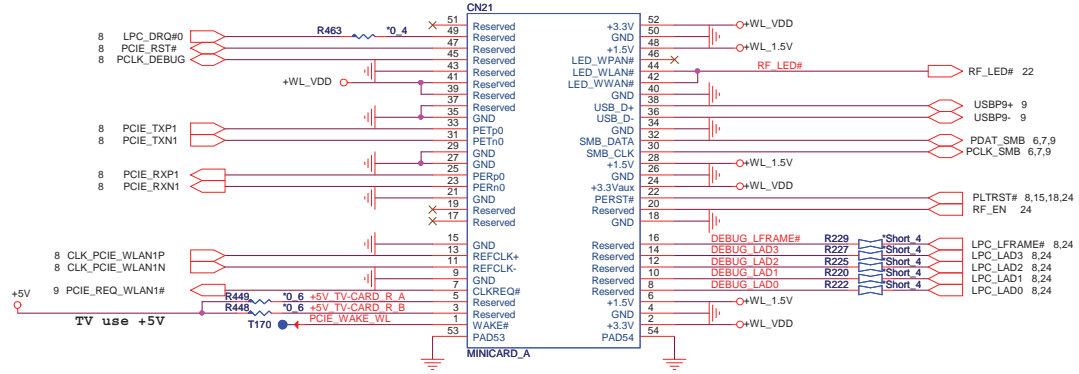
change RJ45 connector without LED
03/02

We will change RJ45 connector

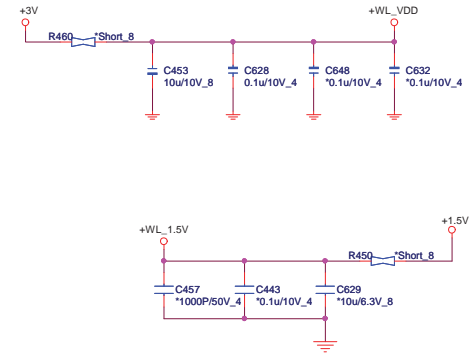
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



Debug



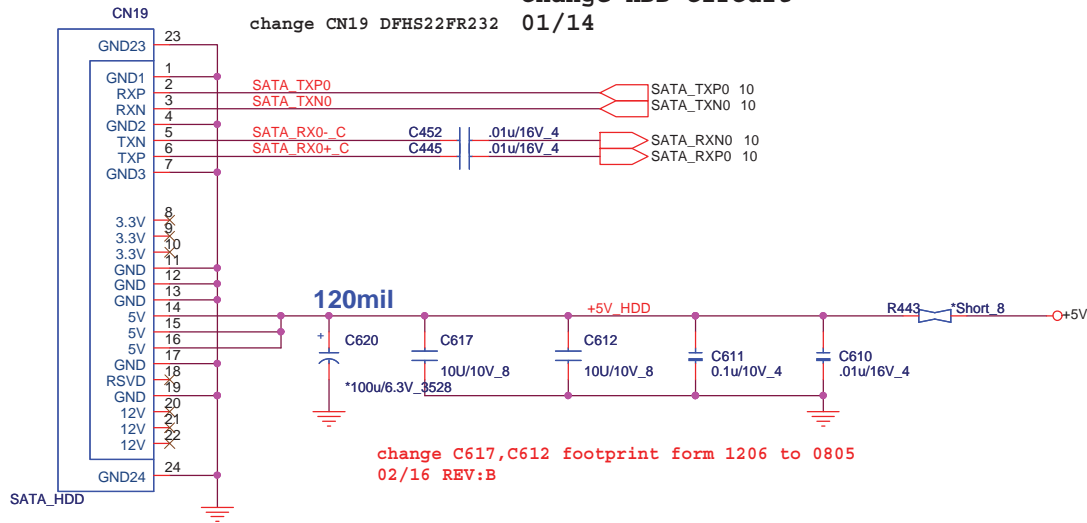
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI-E card	1A
Date:	Tuesday, March 15, 2011	Sheet 16 of 32

SATA HDD

change HDD circuit

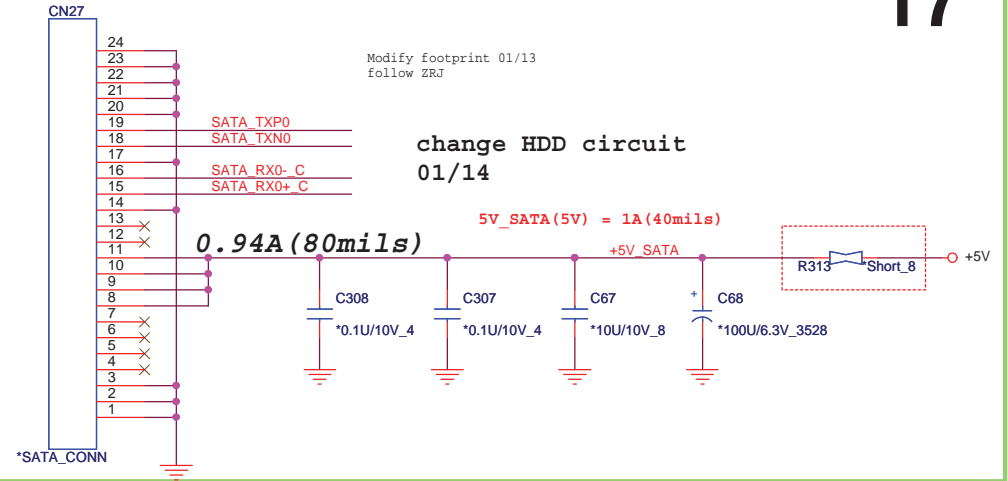
change CN19 DFHS22FR232 01/14



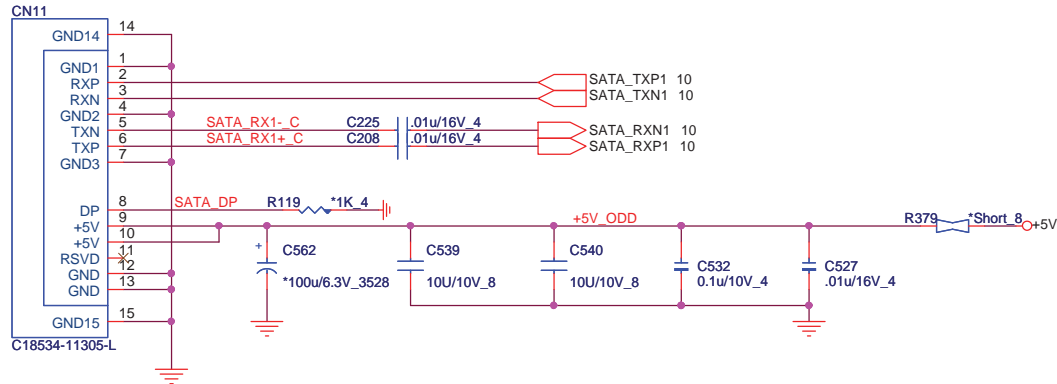
SATA HDD(HDD)

Modify footprint 01/13
follow ZRJ

change HDD circuit
01/14



SATA ODD



PROJECT : ZQP
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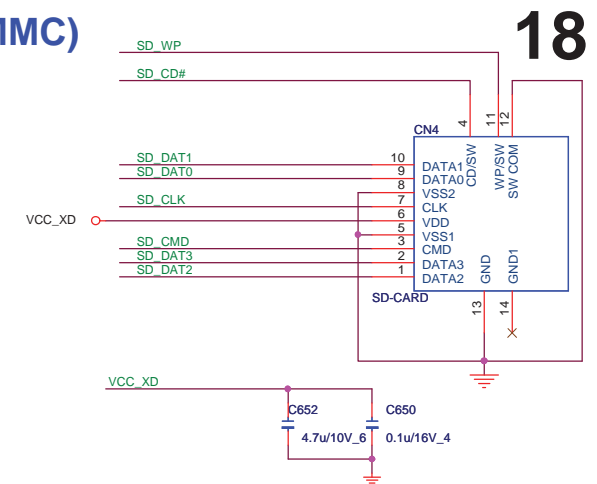
Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

Date: Tuesday, March 15, 2011 Sheet 17 of 32

CARD READER Controller AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

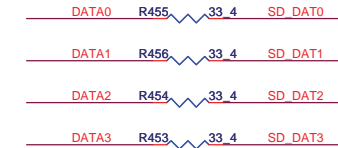
Main	DFHS11FR011
Second	DFHS11FR033



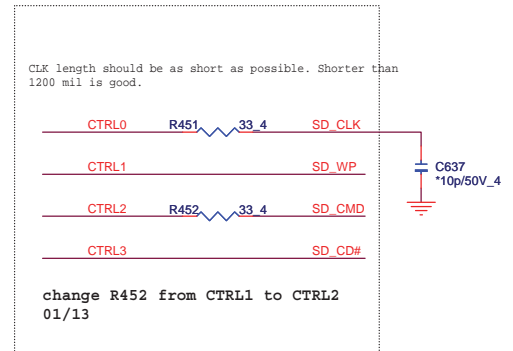
Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

CTRL0, CTRL1 trace length shorter ,
and surround with GND.

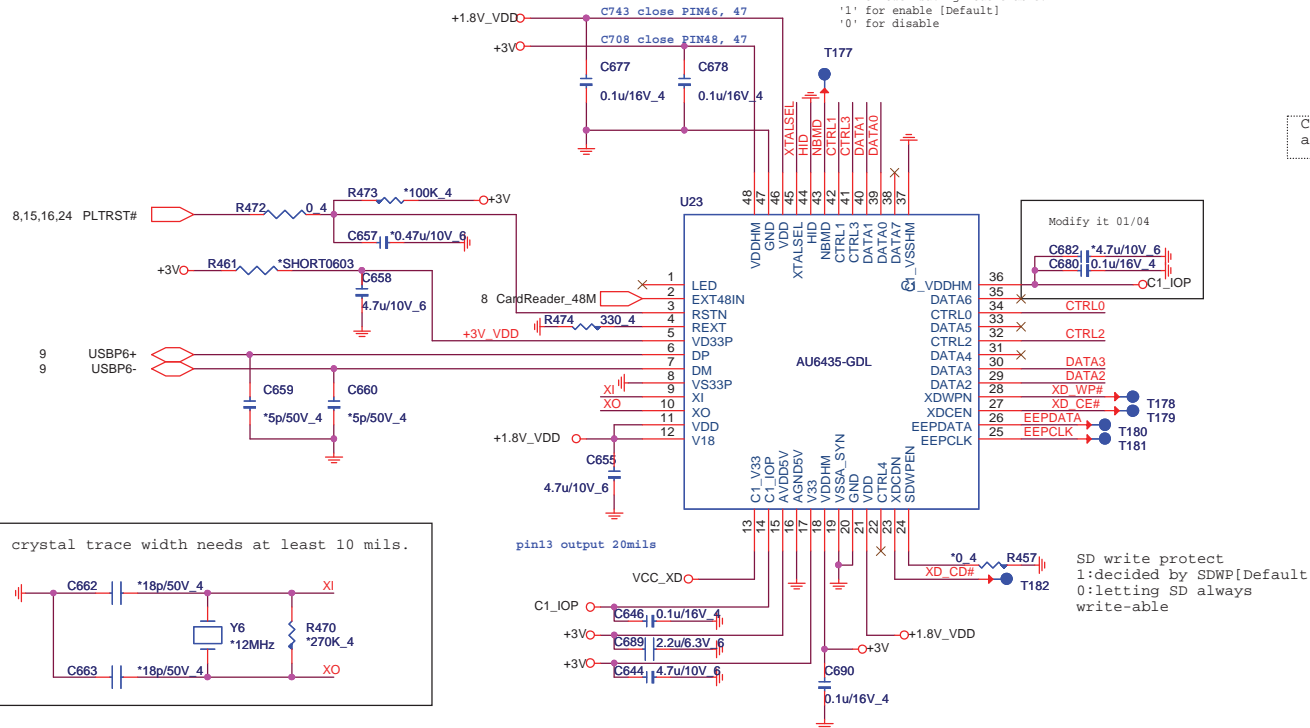
The trace length difference for each card interfaces should be
smaller than 500 mil



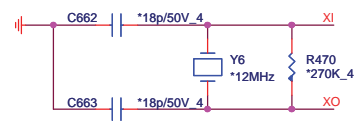
Close to connector



change R452 from CTRL1 to CTRL2
01/13



crystal trace width needs at least 10 mils.



SD write protect
1:decided by SDWP[Default]
0:letting SD always
write-able



PROJECT : ZQP
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Size	Document Number	Rev
	AU6435 CardReader	1A
Date:	Tuesday, March 15, 2011	Sheet 18 of 32

Port Configuration

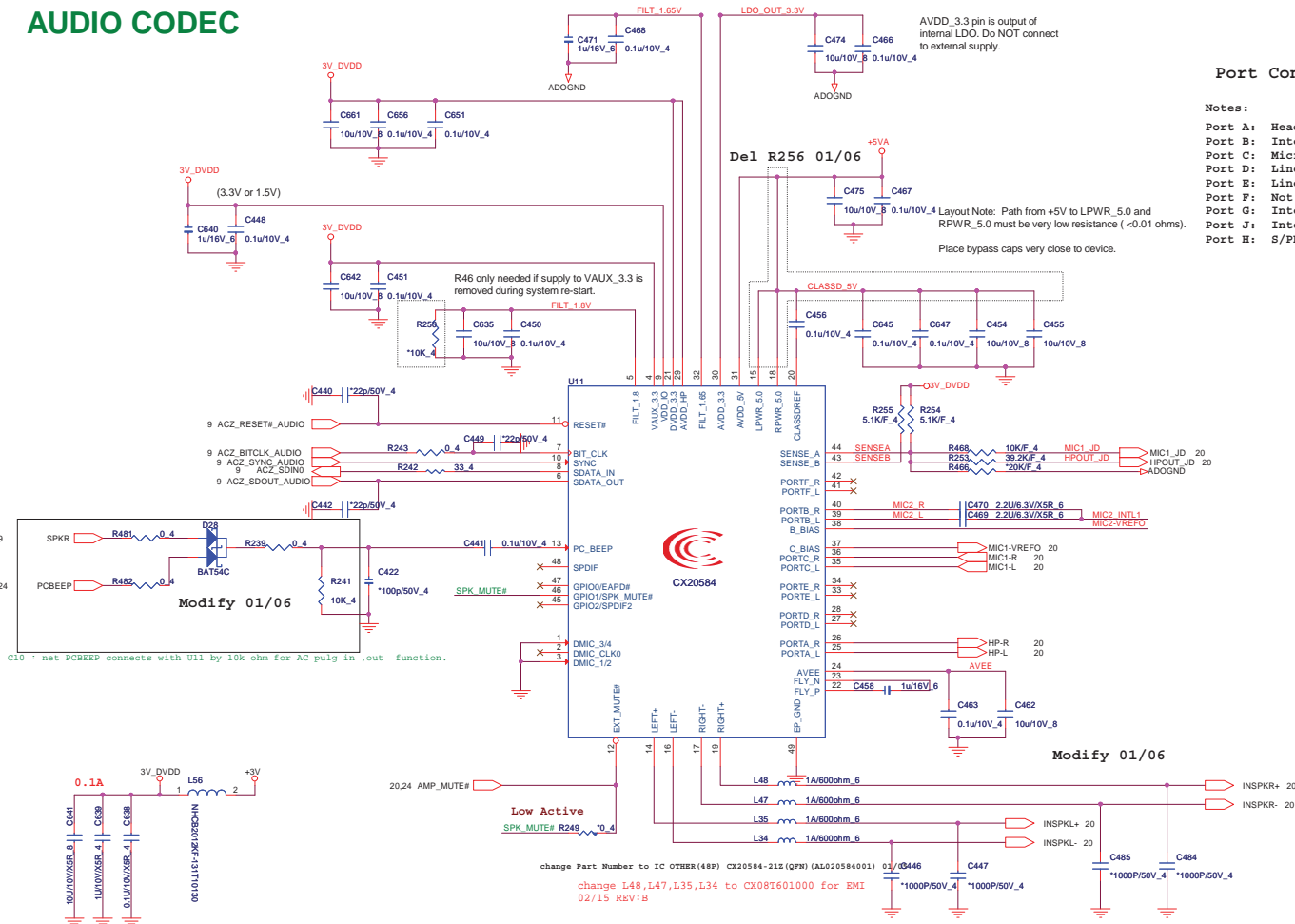
Notes:

- Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

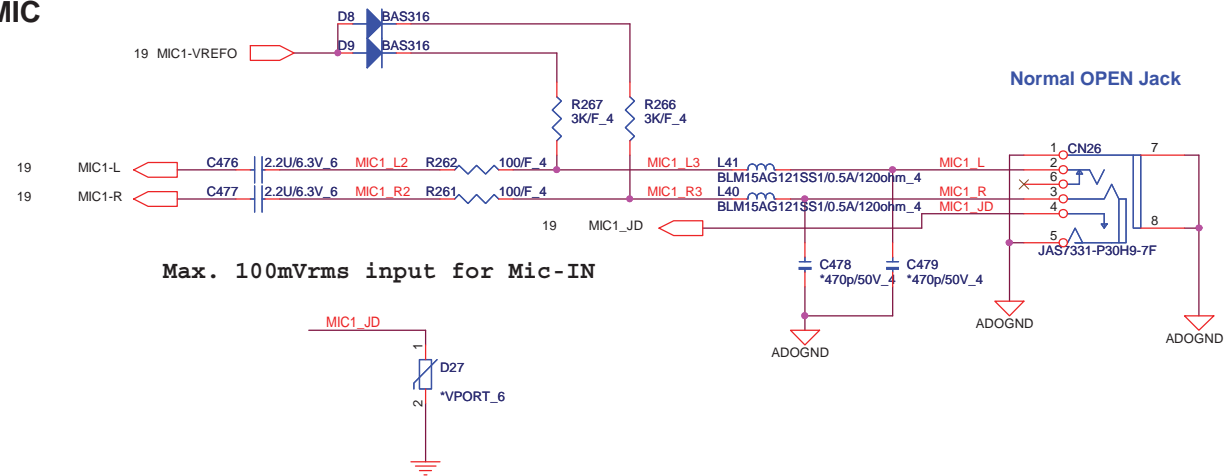
Del R256 01/06

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

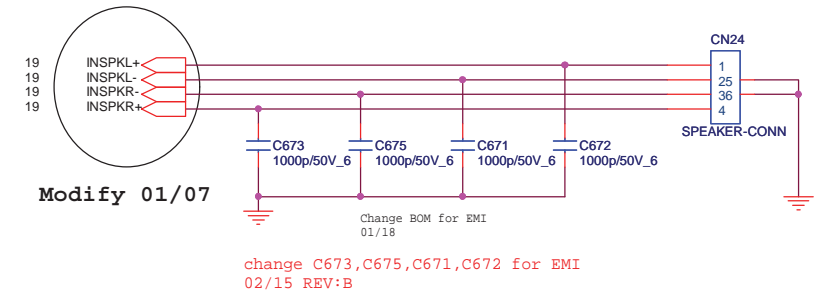
4 Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



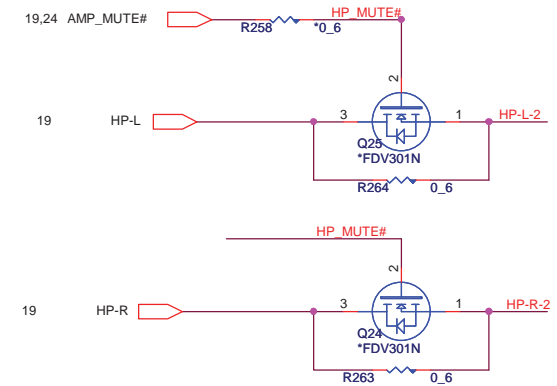
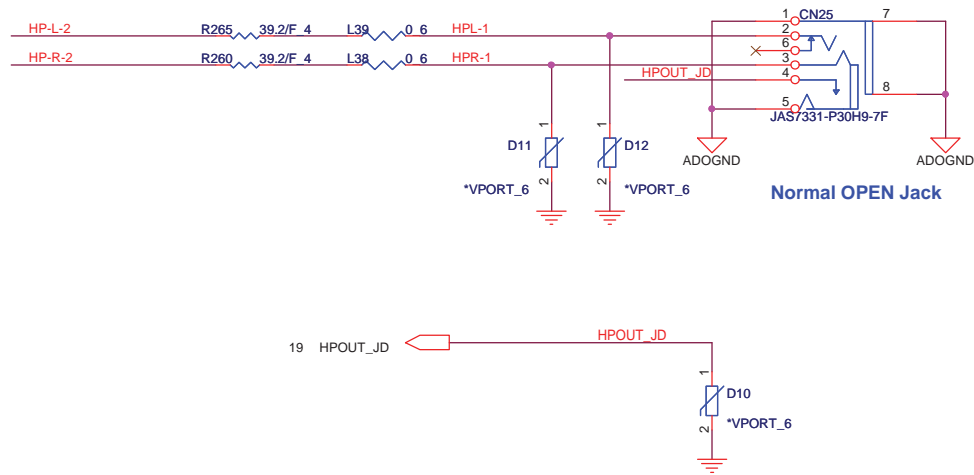
MIC



Internal Speaker



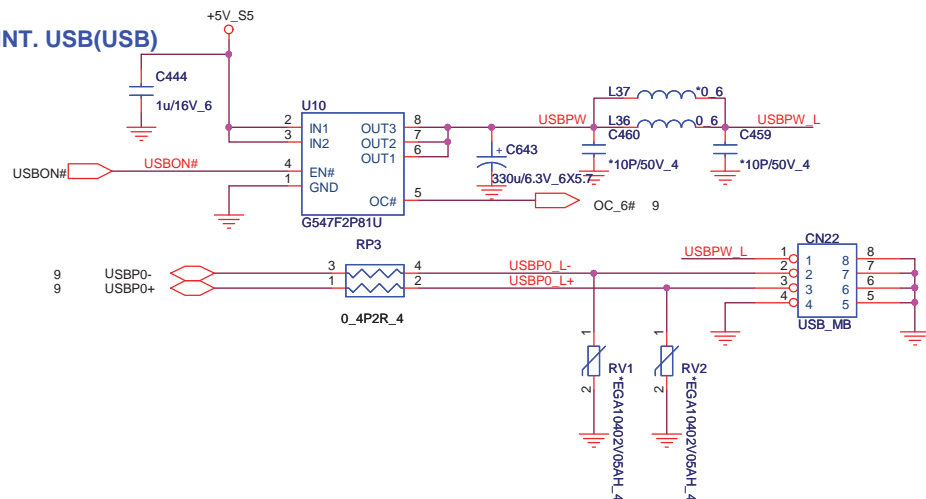
HP



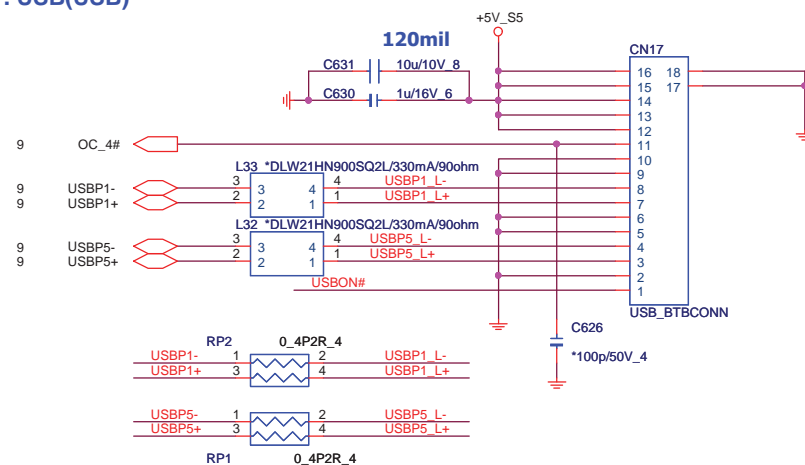
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO JACK CONN	1A
Date:	Tuesday, March 15, 2011	Sheet 20 of 32

INT. USB(USB)

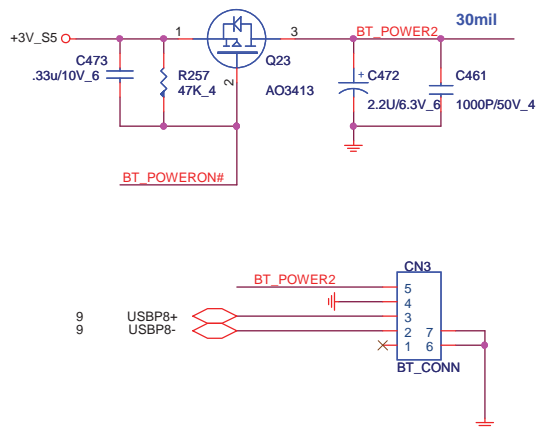


EXT. USB(USB)

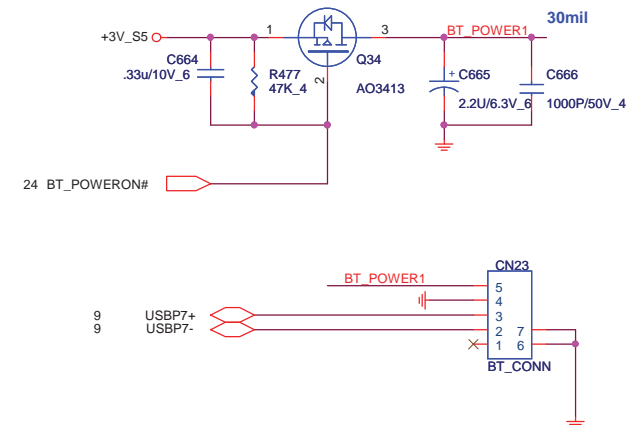


21

BLUETOOTH V2.1 CONN(BTM)



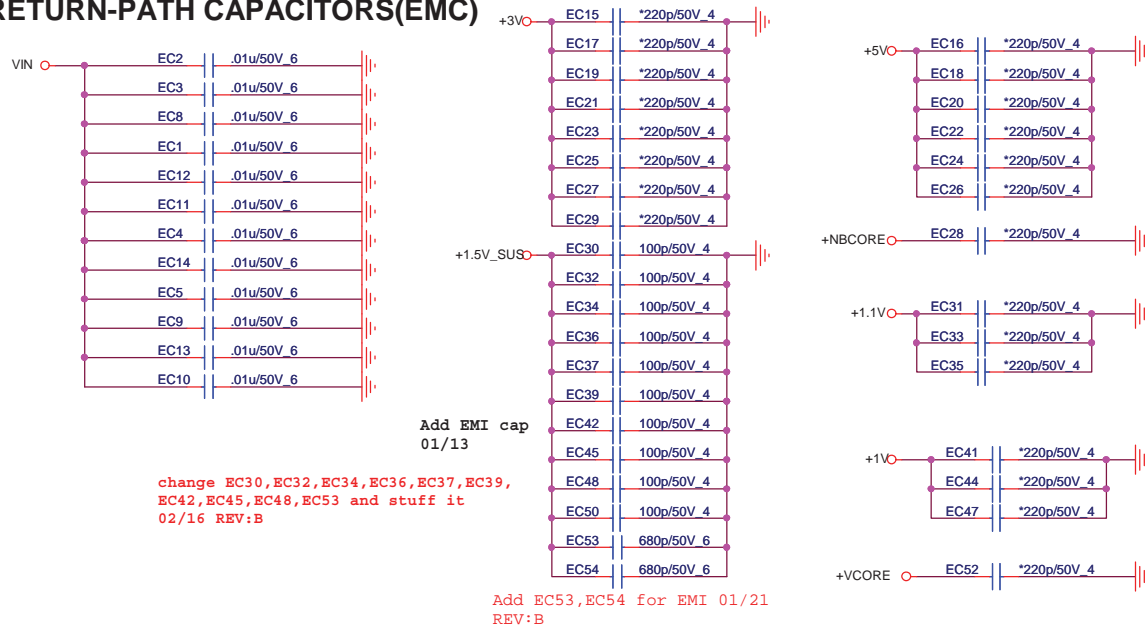
BLUETOOTH V3.0 CONN(BTM)



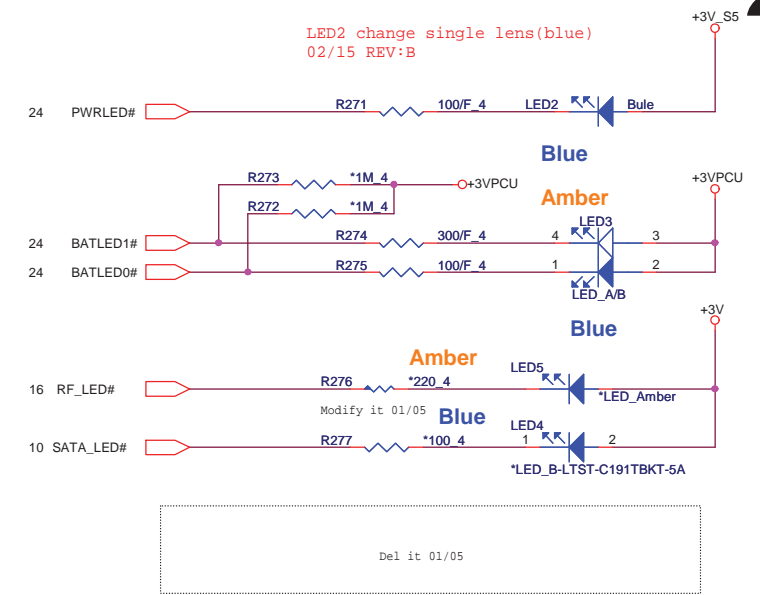
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number USB/BT	Rev 1A
Date:	Tuesday, March 15, 2011	Sheet 21 of 32

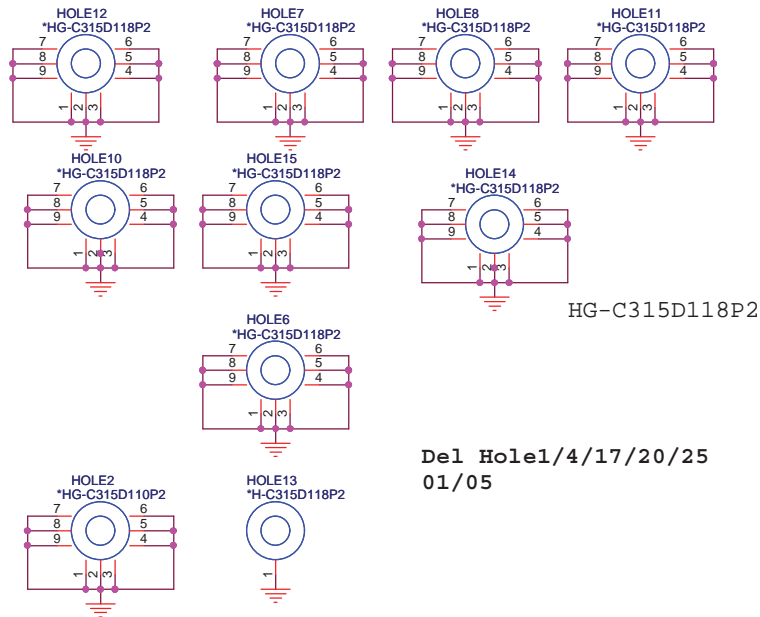
EE RETURN-PATH CAPACITORS(EMC)



LED(UIF)



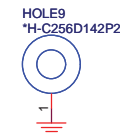
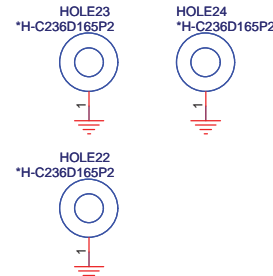
HOLE(OTH)



mini PCI



cpu



No stuff HOLE9
REV:B 02/17

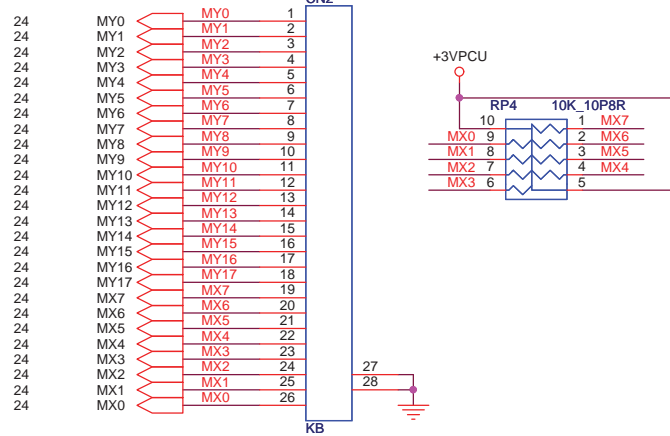
CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3



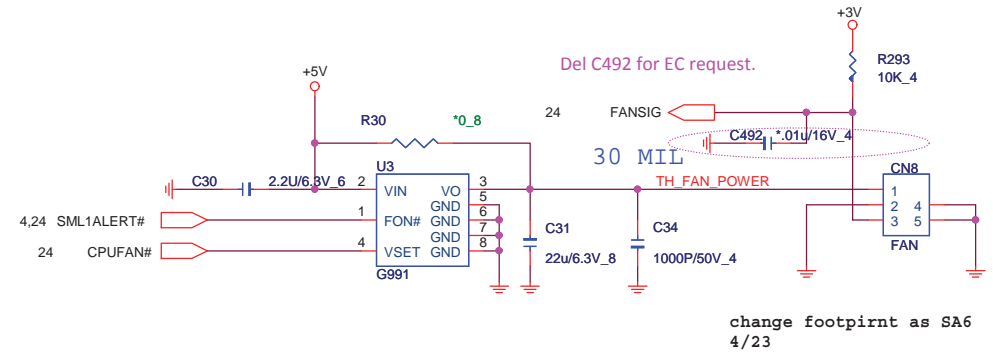
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	LED/ EMI/ Screw Hole& Nut	1A
Date:	Tuesday, March 15, 2011	Sheet 22 of 32

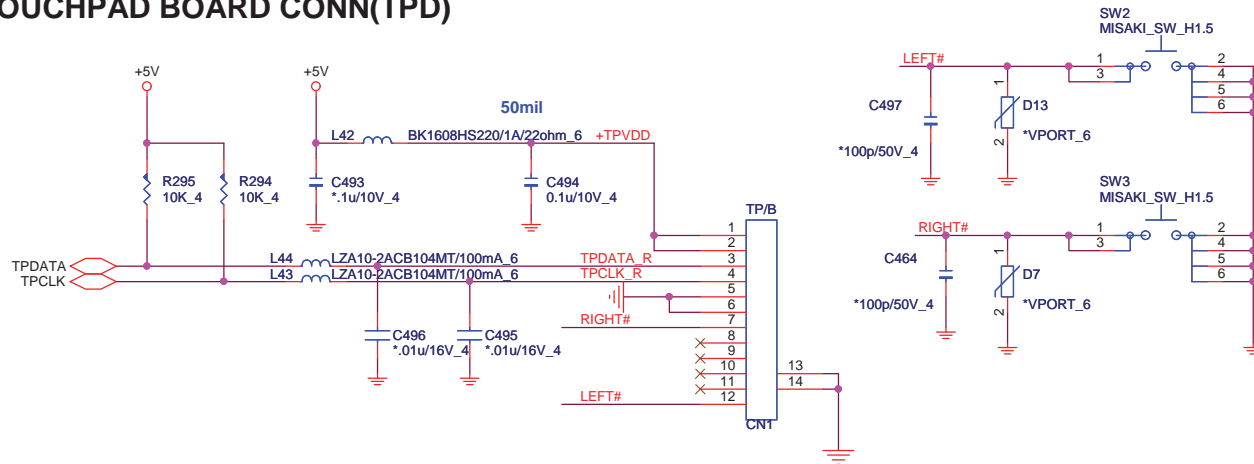
K/B(KBC)



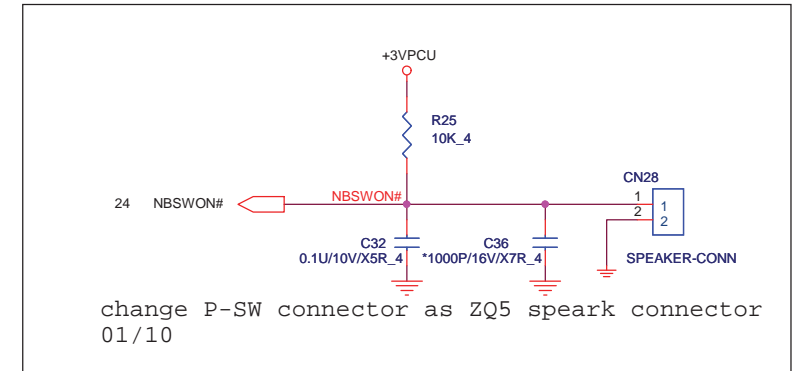
CPU FAN(THM)



TOUCHPAD BOARD CONN(TPD)



DFFC12FR234 will be EOL by PDC , so change PN to DFFC12FR026

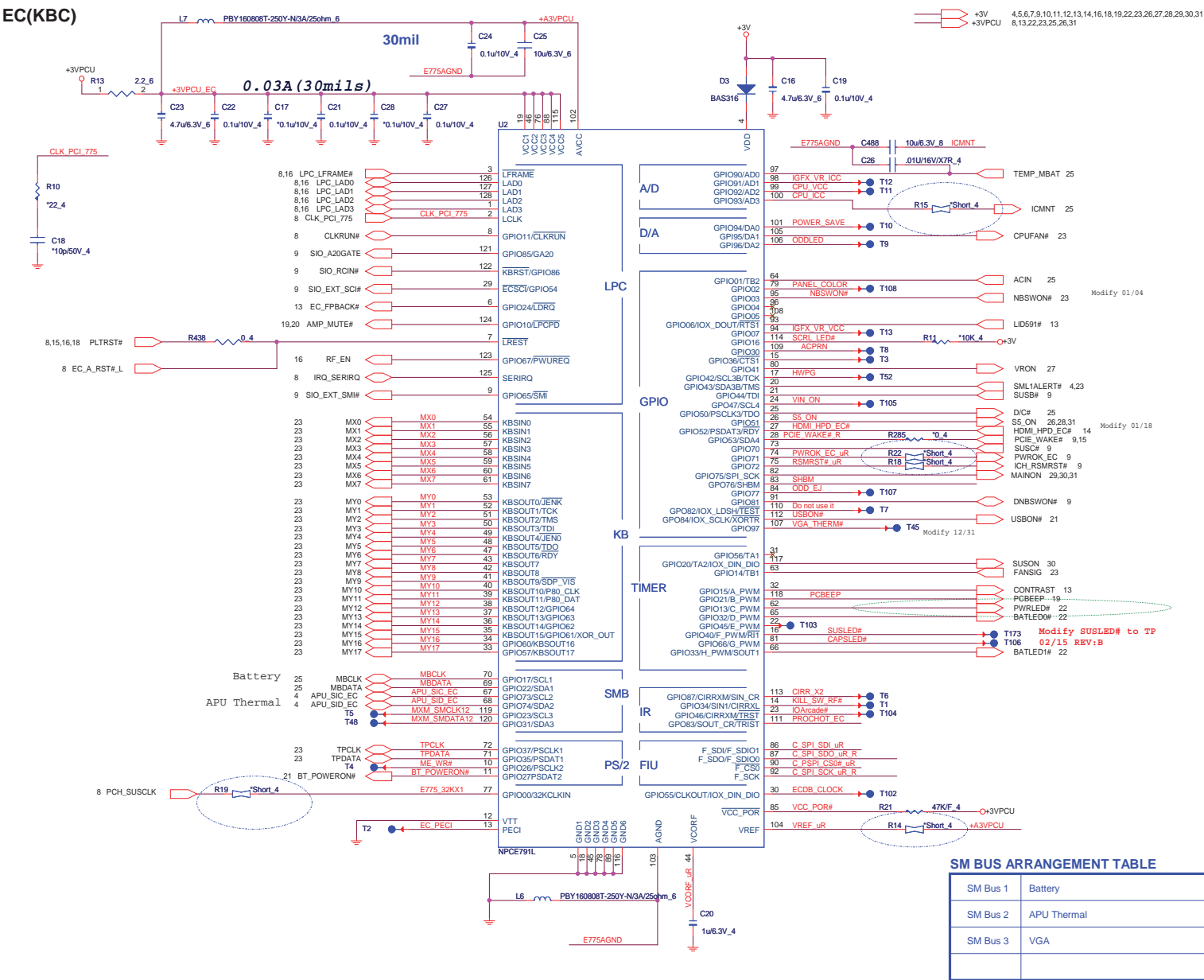


change P-SW connector as ZQ5 speak connector
01/10



PROJECT : ZQP
Quanta Computer Inc.

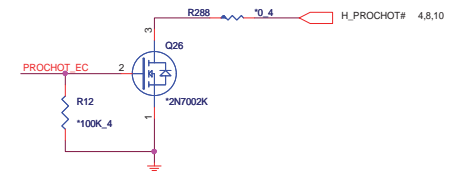
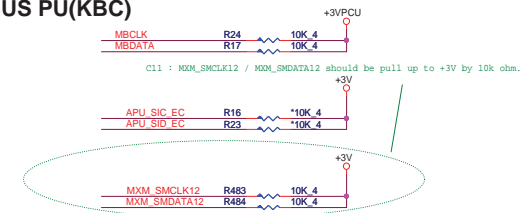
Size	Document Number	Rev
	KB/TP/FAN	1A
Date:	Tuesday, March 15, 2011	Sheet 23 of 32



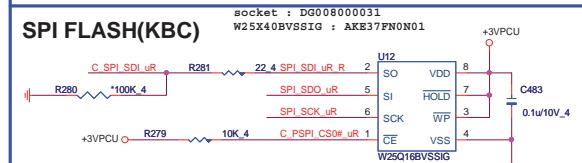
I/O ADDRESS SETTING(KBC)



SM BUS PU(KBC)

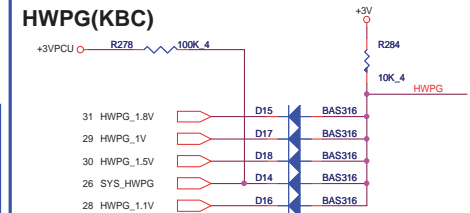


SPI FLASH(KBC)

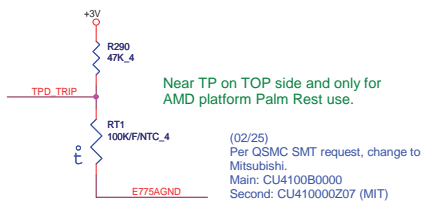


1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

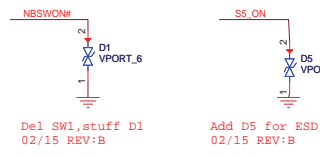
HWPG(KBC)



PALM REST THERMAL SENSOR (THM)



POWER-ON SWITCH (KBC)



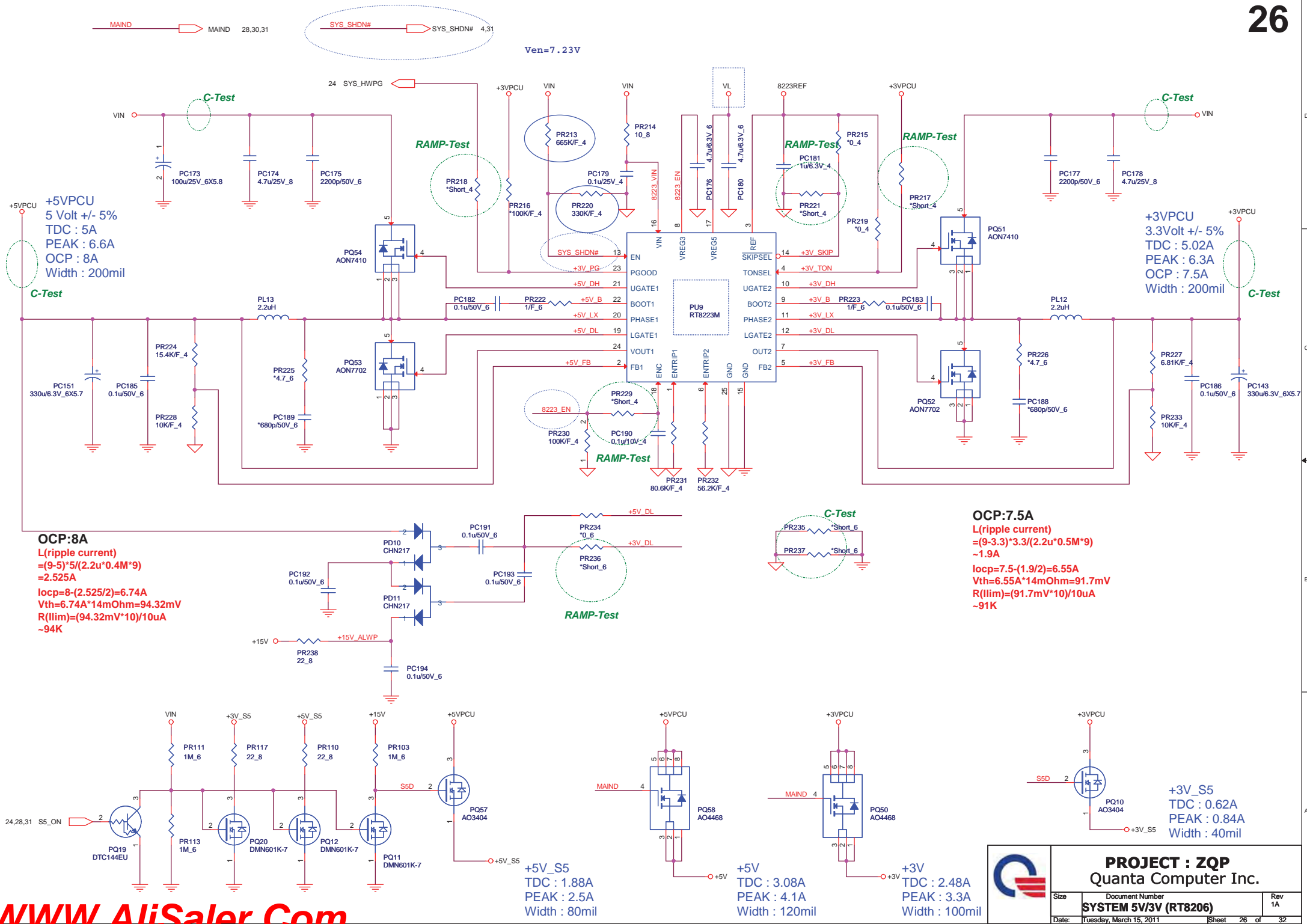
SM BUS ARRANGEMENT TABLE

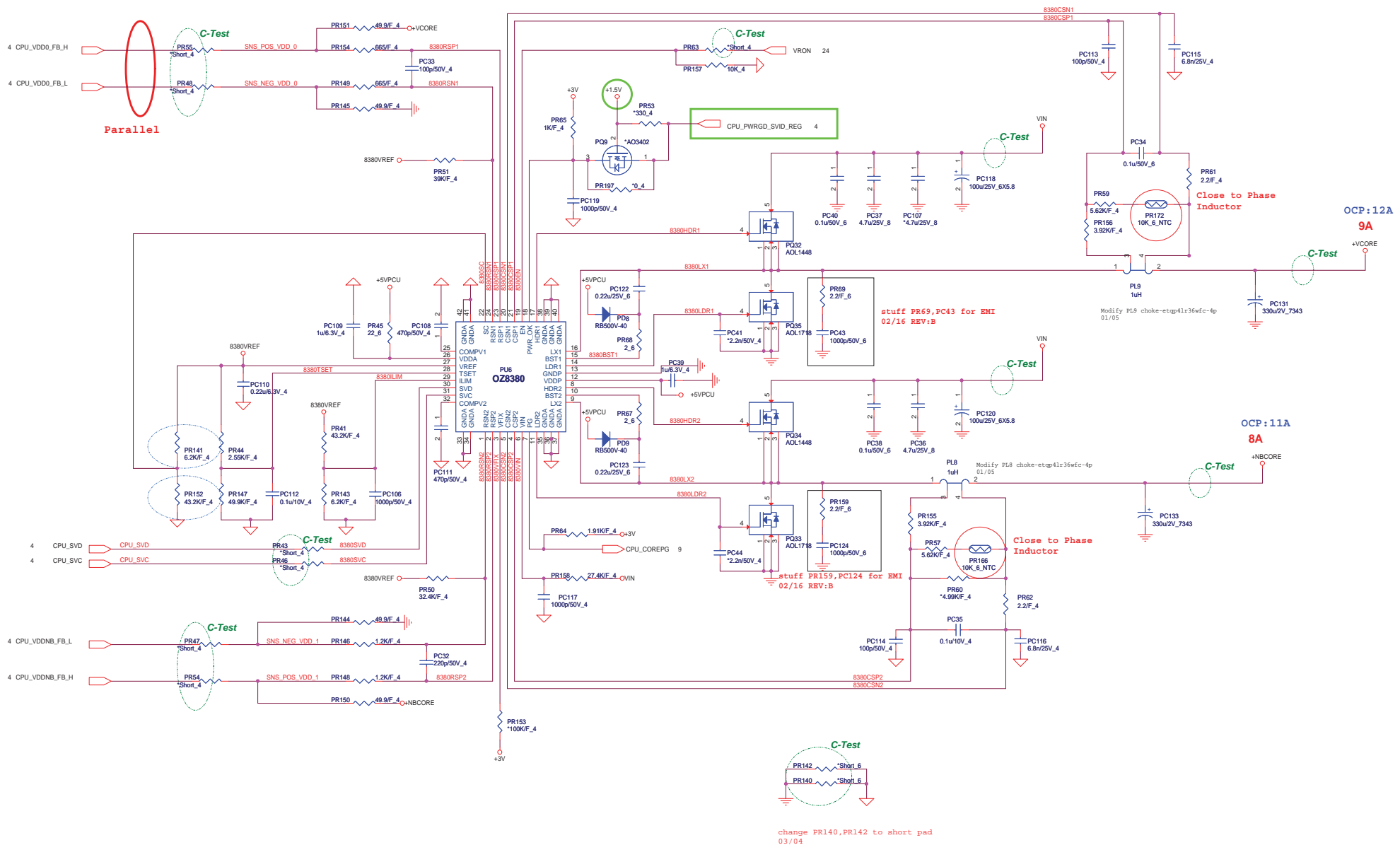
SM Bus 1	Battery
SM Bus 2	APU Thermal
SM Bus 3	VGA

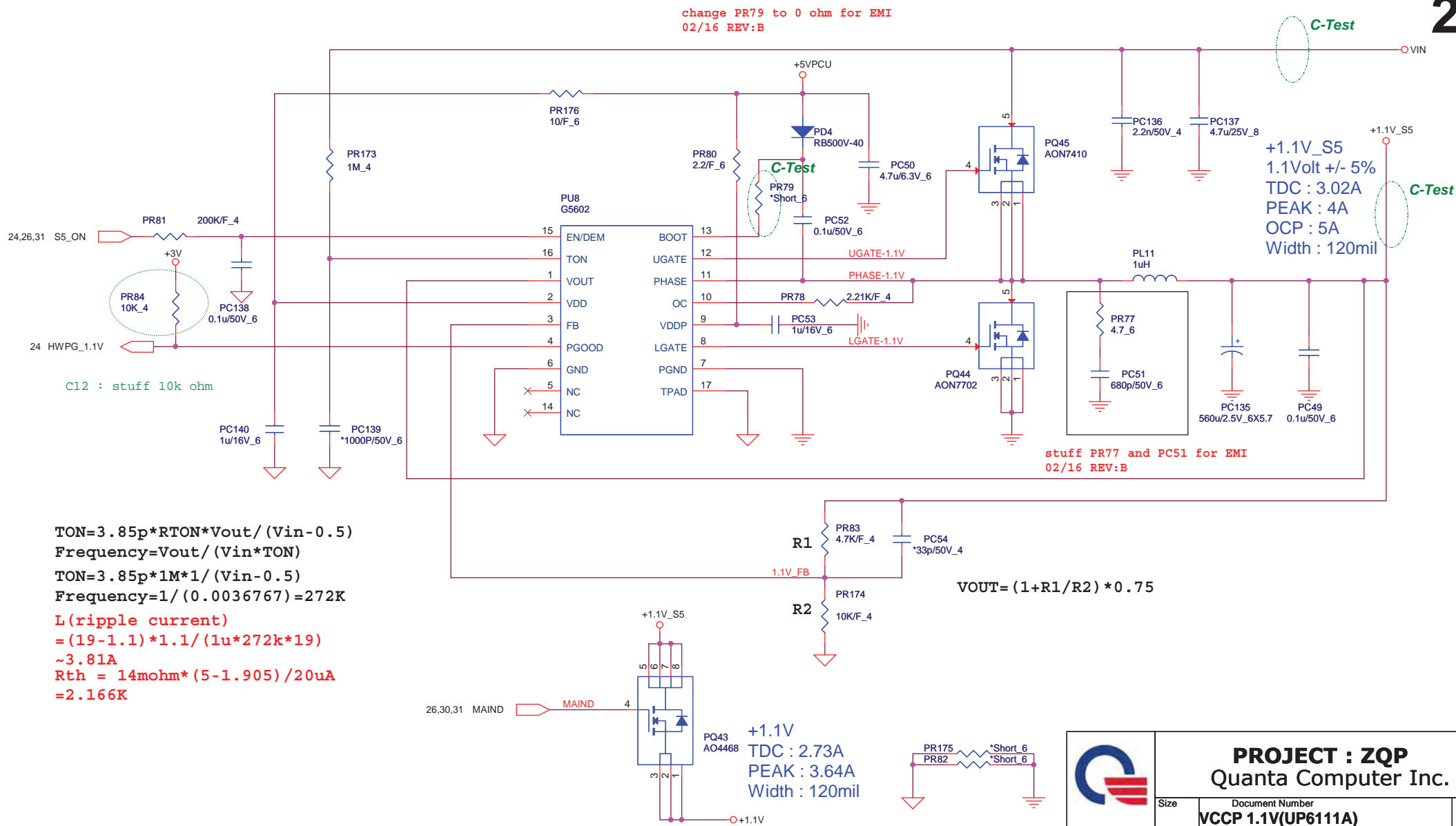


PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number WPCE791 & FLASH	Rev 1A
Date:	Tuesday, March 15, 2011	Sheet 24 of 32

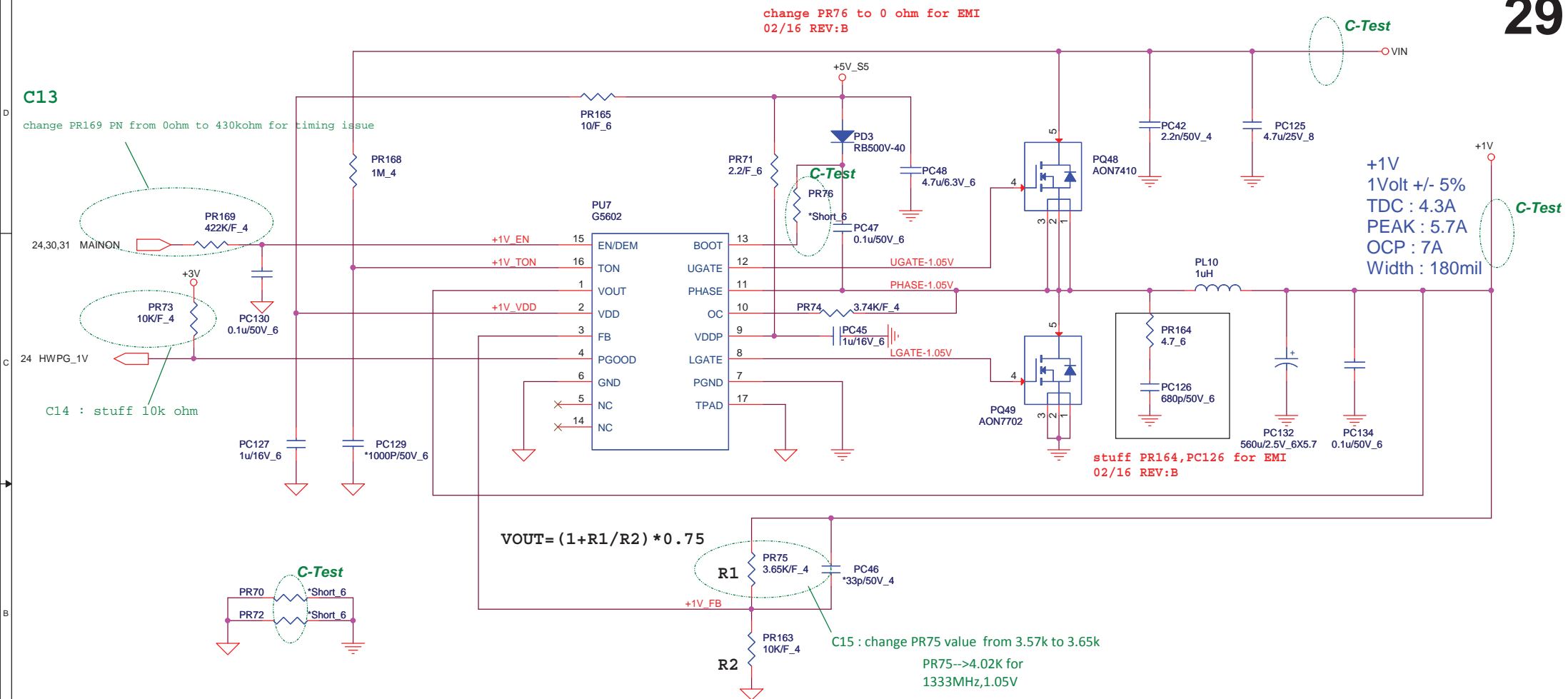






PROJECT : ZQP
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Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
Date:	Tuesday, March 15, 2011	Sheet 28 of 32



$$\text{TON} = 3.85 \mu\text{s} \cdot \text{RTON} \cdot \text{Vout} / (\text{Vin} - 0.5)$$

$$\text{Frequency} = \text{Vout} / (\text{Vin} \cdot \text{TON})$$

$$\text{TON} = 3.85 \mu\text{s} \cdot 1\text{M} \cdot 1 / (\text{Vin} - 0.5)$$


$$\text{Frequency} = 1 / (0.0036767) = 272\text{K}$$

$$L(\text{ripple current}) = (19 - 1) \cdot 1 / (1 \mu\text{s} \cdot 272\text{k} \cdot 19)$$

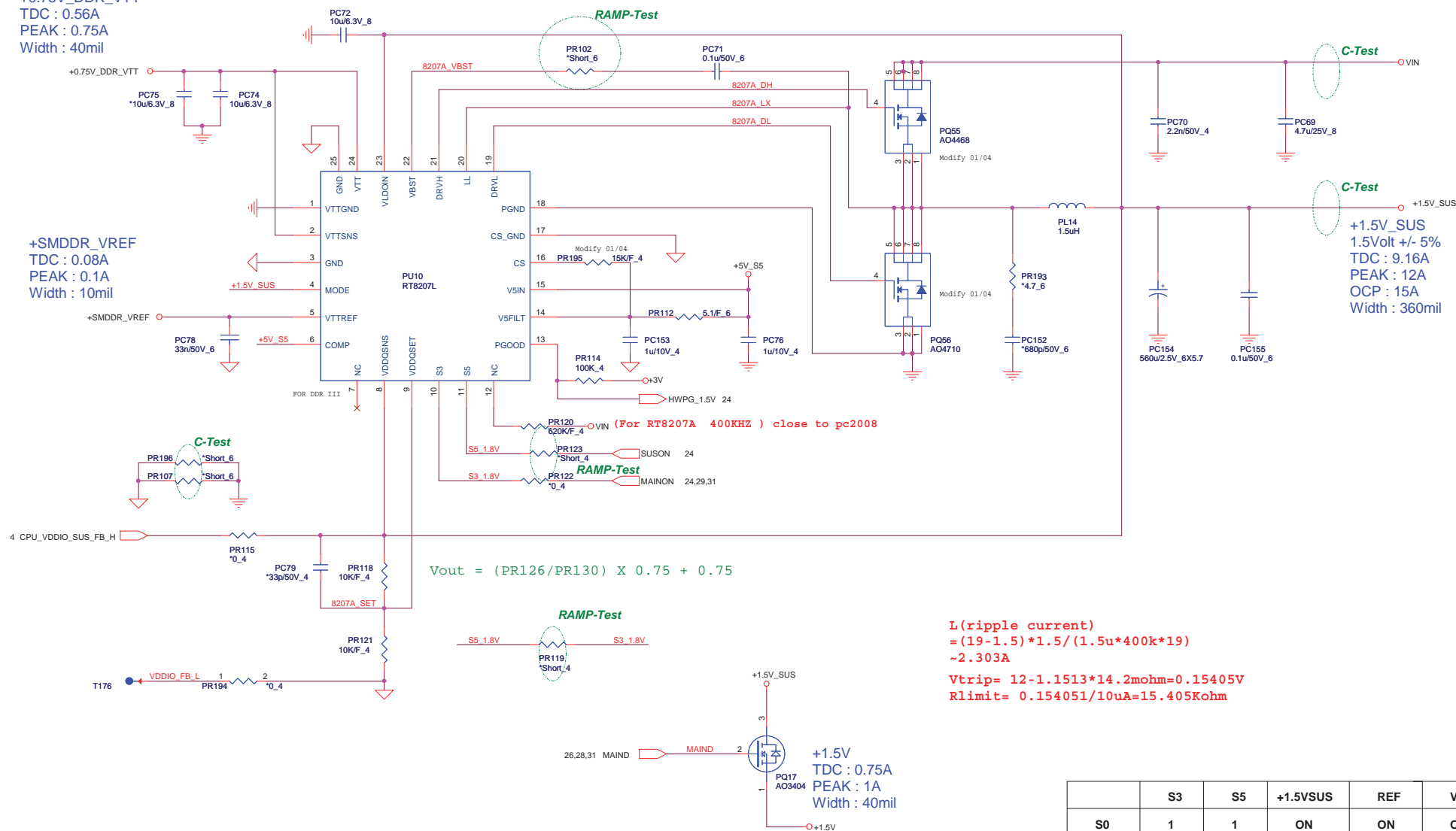
$$\sim 3.483\text{A}$$

$$R_{th} = 14\text{mohm} \cdot (10 - 1.741) / 20\mu\text{A}$$

$$= 3.68\text{Kohm}$$

		PROJECT : ZQP	
		Quanta Computer Inc.	
Size	Document Number	Rev 1A	
	+1V(G5602)		
Date:	Tuesday, March 15, 2011	Sheet	29 of 32

+0.75V_DDR_VTT
TDC : 0.56A
PEAK : 0.75A
Width : 40mil



$$V_{out} = (PR126/PR130) \times 0.75 + 0.75$$

```
L(ripple current)
=(19-1.5)*1.5/(1.5u*400k*19)
~2.303A

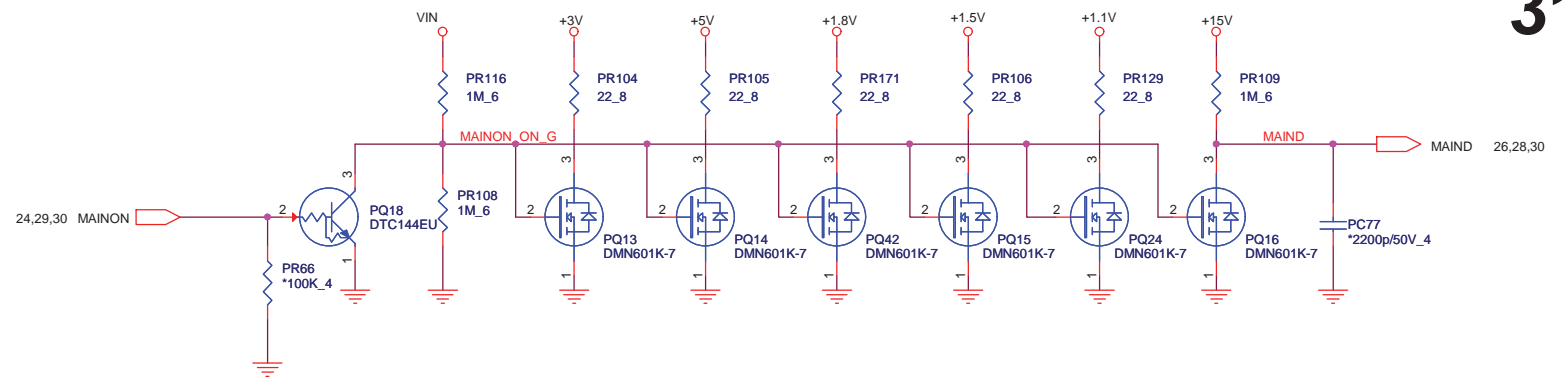
Vtrip= 12-1.1513*14.2mohm=0.15405V
Rlimit= 0.154051/10uA=15.405Kohm
```

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

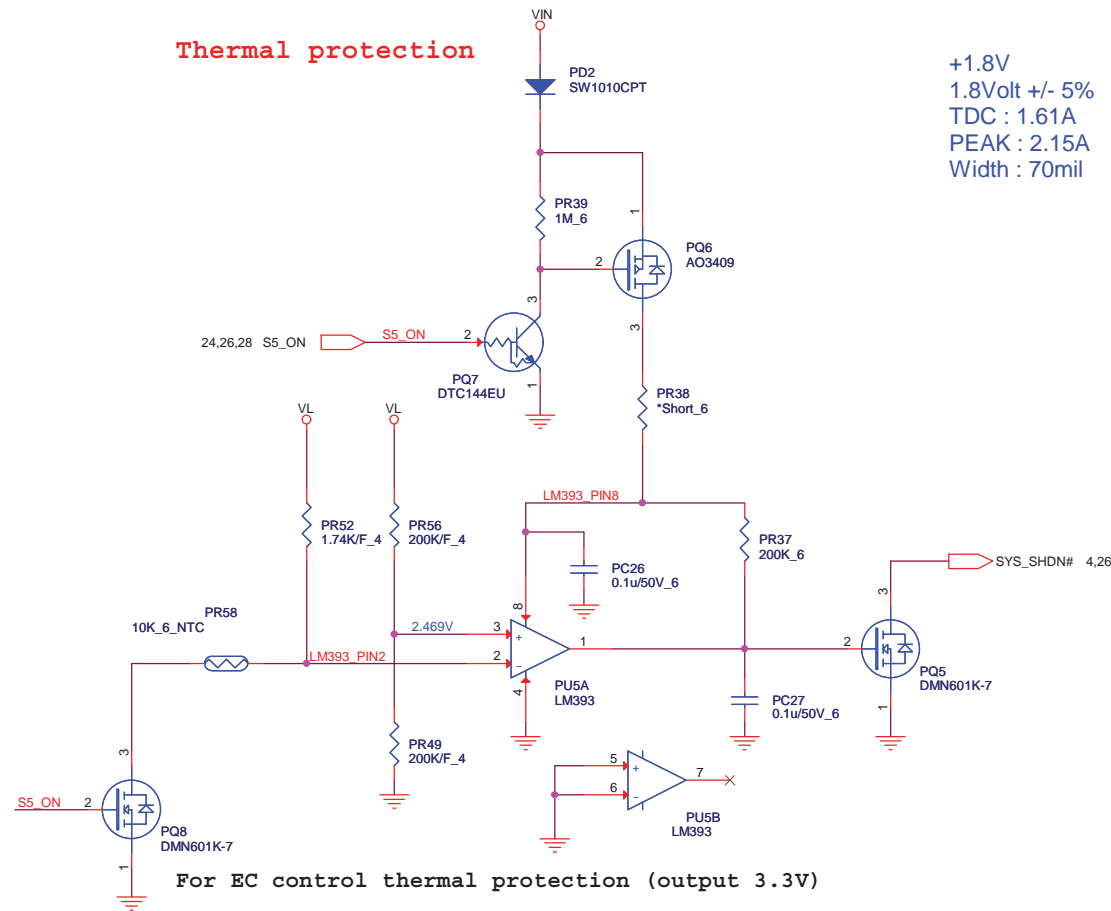


PROJECT : ZQP
Quanta Computer Inc.

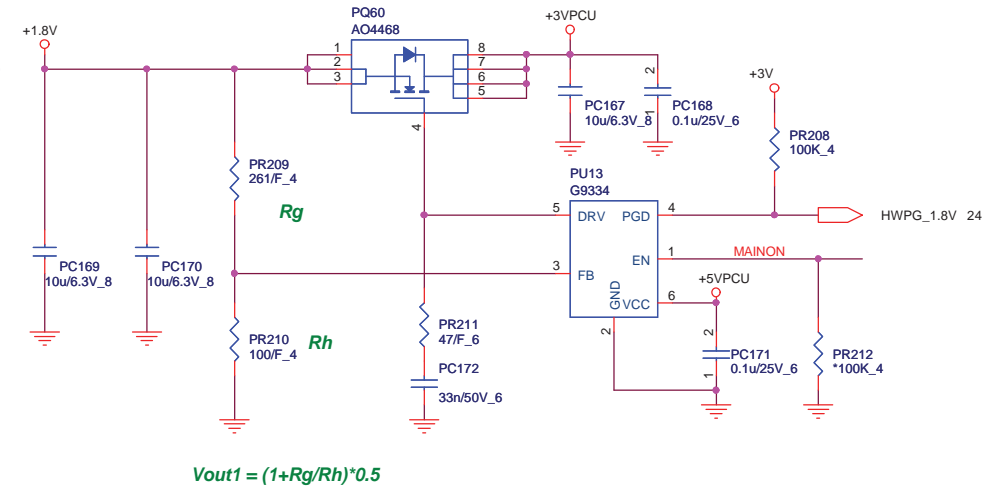
Size	Document Number DDR 1.5V(TPS51116)	Rev 1A
Date:	Tuesday, March 15, 2011	Sheet 30 of 32



Thermal protection




+1.8V
1.8Volt +/- 5%
TDC : 1.61A
PEAK : 2.15A
Width : 70mil



PROJECT : ZQP
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Size	Document Number	Rev
	Discharge /Thermal protection	1A
Date:	Tuesday, March 15, 2011	Sheet 31 of 32

MODEL	REV	CHANGE LIST	Model ZQE/G M/B BOARD			
			Page	From	To	
ZQP/Q M/B	A	First Release	1	1A	3A	
			2	1A	3A	
			3	1A	3A	
<div>01.P14: Add HDMI function 02.P22: Add EC53,EC54 for EMI 03.P20: Stuff C673/C675/C671/C672 for EMI 04.P15: Stuff ESD protector at R31/R32 for EMI 05.P10: GPIO 58 define to HDMI strap pin 06.P08: Add C606,C614,C619 for strong clock 07.P20:change C673,C675,C671,C672 for EMI 08.P19:change L48,L47,L35,L34 to CX08T601000 for EMI 09.P24:No stuff SW1,stuff D1 10.P24:Add D5 on S5_ON for ESD 11.P22:LED2 change single lens(blue) 12.P08:Del C623 13.P24:Del SW1 14.P13:Del R26,R27 and add RP5 for EMI 15.P15:Add EC38,EC40,EC43,EC46 for EMI 16.P28:change PR79 to 0 ohm and stuff PR77 and PC51 for EMI 17.P29:change PR76 to 0 ohm and stuff PR164,PC126 for EMI 18.P27:stuff PR69,PC43 for EMI 19.P17:change C617,C612,C539,C540 footprint form 1206 to 0805 20.P13:Swap USB nets between L50 and PR5 21.P13:Add R33,R34 for ESD 22.P15:change C354 to CH122GK1110 for EMI 23.P22:change EC30,EC32,EC34,EC36,EC37,EC39,EC42,EC45,EC48,EC53 and stuff it for EMI 24.P26:Remove JP20,JP21,JP22,JP23 and change to short pad PR235,PR237 25.P27:Remove JP10,JP9,JP6,JP8 and change to short pad PR55,PR48,PR43,PR46,PR47,PR54,PR63,PR142,PR140 26.P28:Remove JP24,JP25 27.P29:Remove JP16,JP17 and change to short pad PR70,PR72 28.P30:Remove JP18,JP19 and change to short pad PR196,PR107 29.P22:No stuff HOLE9</div>	B	4	1A	3A		
		5	1A	3A		
		6	1A	3A		
		7	1A	3A		
		8	1A	3A		
		9	1A	3A		
		10	1A	3A		
		11	1A	3A		
		12	1A	3A		
		13	1A	3A		
		14	1A	3A		
		15	1A	3A		
		16	1A	3A		
		17	1A	3A		
		18	1A	3A		
		19	1A	3A		
		20	1A	3A		
		21	1A	3A		
		22	1A	3A		
		23	1A	3A		
		24	1A	3A		
		25	1A	3A		
		26	1A	3A		
		27	1A	3A		
		28	1A	3A		
		29	1A	3A		
		<div>01.P15:change RJ45 connector without LED 02.P27:change PR140,PR142 to short pad 03.P30:change PR119,PR123,PR102 to short pad 04.P26:change PR217,PR218,PR221,PR229,PR236 to short pad 05.P29:change PR76 to short pad 06.P28:change PR79 to short pad</div>	B	30	1A	3A
				31	1A	3A
				32	1A	3A
33	1A			3A		
34	1A			3A		
35	1A			3A		
36	1A			3A		
37	1A			3A		
38	1A			3A		
39	1A			3A		
40	1A			3A		
41	1A			3A		
<div><div></div><div><div>PROJECT : ZQP</div><div>Quanta Computer Inc.</div></div></div>			<div><div>Size</div><div>Document Number</div><div>Rev</div></div> <div><div>CHANGE LIST - 3A</div><div>1A</div></div> <div><div>Date: Tuesday, March 15, 2011</div><div>Sheet 32 of 32</div></div>			
Quanta Computer Inc.		PROJECT: ZQP/Q	PCBA NO.	REV: 3A	DOC. NO :	
APPROVED BY : Andy Lin		CHECK BY : JC Huang	DRAWING BY : Andy Chen		DATE :10/18/2010	SHEET 1